Project 2: Voltage Controlled Oscillator

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William T. Jarratt and Thomas H. Parsons pledges that all work contained within represents their own work and the work of nobody else.

Contents

Abstract

This article describes the design of a 10 GHz CMOS Voltage Controlled Oscillator (VCO), tuned with 2-bit differential band switching and an inversion mode NMOS varactor. The VCO was implemented using the 45 nm CMOS process and is tunable over a 10% range, 9.5 GHz to 10.5 GHz, with a 50% band overlap. The VCO is designed with a power consumption and phase noise that together achieve a figure of merit of less than -170 dB across all bands. The VCO output buffer drives a 50 pF load and is designed as a two stage inverter chain.

1. Specification Table

Table 1 shows the requirements for the voltage controlled oscillator (VCO), along with the results from the design described in this article. Plots or schematics showing the relevant result are also given. Any specifications that require additional explanation are noted with superscript numbers and the explanation is given below the table. Specifications not met have their row highlighted red.

Specifications and Results (With Output Buffer)			
Metric	**Specification**	**Result**	**Shown by**
Frequency Range	10 GHz center with 10% (1 GHz) monotonic tuning range.	Frequency range is 9.483 GHz to 10.502 GHz, 1.019 GHz.	Fig. 9
Figure of Merit (FoM)[1]	< -170 dB at 1 MHz offset across all bands.	Worst case FoM is -170.142 dB.	Fig. 14 - 20
Power Consumption[2]	As needed to hit FoM with Vdd ≤ 2.5 V.	See FoM specification. Vdd of 2.5 V used.	Fig. 1, 14, 23
VCO Gain (K_{VCO})[3]	< 0.25 GHz/V across the entire range.	Best case K_{VCO} is 362.81 MHz/V.	Fig. 10
Band Overlap[4]	> 50% (if using bands).	Smallest overlap is 52.28%.	Fig. 9
Output Swing	1.0 Vppd (peak-to-peak differential).	Worst case output swing is 4.66 Vppd.	Fig. 11 - 13
Load Capacitance	50 fF for each side for output of VCO buffer.	Load capacitance is included at buffer output.	Fig. 3, 25

Table 1: Specifications for voltage controlled oscillator along with the results of the design.

1. FoM is calculated using: `((rfOutputNoise("dBc/Hz" ?result "pnoise") - dB20((1e+10 / 1000000.0))) + dB10(((average(IT("/V0/PLUS")) * average(VT("/net2"))) / -0.001)))`
2. Power Consumption is calculated using: `-1 * (average(IT("/V0/PLUS")) * average(VT("/net2")))`
3. VCO Gain is calculated using: `deriv(harmonic(xval(getData("vop" ?result "pss_fd")) '1))`
4. VCO Frequency is calculated using: `harmonic(xval(getData("vop" ?result "pss_fd")) '1)`. The band overlaps are shown below, with the smallest band overlap being 52.28%.

Band	**Low Band - High Band**	**Band Bandwidth [GHz]**	**Overlap Bandwidth [GHz]**	**Percent Band Overlap [%]**
0	0-1	0.39684	0.22927	57.77
1	0-1	0.42014	0.22927	54.56
1	1-2	0.42014	0.23361	55.60
2	1-2	0.44681	0.23361	52.28
2	2-3	0.44681	0.25710	57.54
3	2-3	0.47570	0.25710	54.04

2. Designer Contributions

William and Thomas had already built the VCO up to the point of bandswitch capacitors before joining forces and choosing William's target frequency.

- William T. Jarratt
    - Provided initial differential amplifier and current mirror with proper sizing due to choosing 10 GHz as the target frequency.
    - Designed the varactor testbench. Designed the NMOS inversion mode varactor and differential bandswitches. Was responsible for tweaking varactor and bandswitch values to achieve tuning range and band overlaps.
    - Setup S-parameter testbench analysis to report K_{VCO} and VCO Frequency versus control voltage.
    - Responsible for all required plots in the report.
- Thomas H. Parsons
    - Helped debug William's initial 10 GHz VCO design. Weird issue with varactor tuning that was found to be an improperly designed varactor.
    - Designed the two stage inverter output buffer. Tweaked buffer and PMOS/NMOS differential pairs to achieve proper biasing condition and a smooth PSS transient response.
    - Investigated and implemented the tail resistor in place of the current mirror to help with phase noise.
    - Setup analysis to plot average power and figure of merit from PSS analysis.
    - Responsible for all required schematics in the report.
- Both team members
    - Setup VCO testbench to simultaneously perform PSS and S-parameter analysis. Setup K_{VCO} and VCO Frequency versus control voltage for PSS analysis.
    - Incrementally improved figure of merit by running a noise summary and then tweaking transistor sizes to eliminate the top contributors of noise. Thomas did the initial analysis and was able to get the figure of merit within a few dB of the target for all bands. William then continued with tweaking transistor sizes until the figure of merit was met across all sweeps. William simultaneously tweaked total tank capacitance as well to ensure tuning range and band overlap were met.

3. Design Overview

The design was based around a differential cross-coupled CMOS VCO. As shown in figure 4, a cross-coupled PMOS pair was placed at the top, and at the bottom, an NMOS pair. They were sized to have low flicker noise and for a DC voltage of about Vdd/2 at the differential outputs of the VCO. A voltage drop across the bottom resistor generated the current through the VCO circuit. An ideal current source was not used. The resistor generated significantly less noise than a simple current mirror, and it helped achieve a figure of merit less than -170 dB across all bands. The LC tank circuit responsible for the oscillations is shown in figure 5. The tank consisted of a small fixed capacitor, a small startup current, ASITIC extracted inductor, two NMOS varactors, and a capacitor bank. A differential Q of 14.31 was achieved for a 1.558 nH inductor. The pi network model for the ASITIC inductor and a single NMOS varactor are shown in figure 6. The capacitor bank has 2 bits which results in 4 bands total. Only 2 bits were needed to achieve greater than 50% band overlap for all bands. The band switches were differential with component values that were either scaled up or down by a factor of 2 as shown in figure 8. A buffer consisting of two CMOS inverters connected to each of the VCO differential outputs in order to drive the required 50 fF load.

4. Design Methodology

1. The first step should be to set up the initial PMOS/NMOS cross-coupled differential amplifier with a tank circuit that contains a fixed capacitor and ideal inductor with a parasitic resistor scaled for the VCO frequency and the target inductor Q value. The cross-coupled differential amplifier has a single stage current mirror to control the current biasing of the differential amplifier.
2. The next step is to determine the biasing condition for the circuit.
    a. The initial goal of this step is to get the PSS simulation working, at any frequency. This means paying attention to the g_m of each transistor and also making sure that no transistors are falling out of saturation. The differential amplifier transconductance must exceed the tanks conductance. Watch the transient analysis. The transient analysis should show an underdamped oscillation.
    b. Once the oscillator is oscillating, the tank inductance, tank capacitance and device sizing must be changed to achieve the approximate VCO frequency. Use the fixed capacitor in the tank to determine the range of capacitances needed. The fixed capacitance should be large enough to account for the baseline capacitance added by the varactor, band switches, and output buffers. The fixed capacitance will be lessened as devices are added and acts as a knob for the tuning range later on.
    c. The DC voltage at the output of the cross-coupled differential amplifier must be designed to work with the output buffer. In this design, a two-stage inverter was used and so an output DC voltage of Vdd/2 was desired. Careful sizing of the NMOS/PMOS differential pair can be leveraged to achieve this voltage.
3. There is no strict order here, but this is the order that this design took. Next the varactor and differential band switches are added. At this point, a testbench should be constructed for the varactor and each band switch. This design began with and only has a 2-bit band switch, however to lessen simulation time, it is recommended to start with 2 bits and only increase the number of bits when it is determined that the specifications cannot be met with the current number of bits.
    a. Knowing that 4 bands would be used initially, the vacactor was initially sized to achieve a range of ¼ the overall range. When implementing the varactor, make sure that the entire range of capacitance is within the tuning voltage range. In this design that was 0 V to Vdd = 2.5 V. This means that the varactor capacitance saturates before reaching either end of the tuning voltage range.
    b. Implement two differential bandswitches. Size the band switches so that the ΔC_{bsw} is less than half of that of the varactor, ΔC_{var}, though they will be tweaked later.
    c. Run the PSS simulation and tweak the fixed capacitance, varactor, and band switches so that the tuning range and band overlap specification is met. Due to needing to tune for the figure of merit and K_{VCO}, it is not imperative that the spec is met exactly.
4. Once the DC operating point is selected and the tuning range is set, ASITIC simulations should be performed to ensure that the chosen inductance value and differential Q value can be achieved. It may be desirable to add the ASITIC model early to account for its effects. The inductance value may need to be adjusted later. Check the PSS analysis after adding the ASITIC model and tweak the circuit to account for its effects. For this design, there were two iterations of the ASITIC inductor. The initial value was 750 pH, but did not allow for full tuning range with four bands.

NOTE:

The Q value of the inductor has a large impact on the ability to achieve the figure of merit. It is worth the time to try to achieve a high differential Q. Investigate differential Q values of greater than 15 and determine if nearby inductances are more likely to provide a high Q value while also working in the VCO circuit.

5. At this stage, the tuning range and band overlap are met, however this will need further tweaking as the output buffers are added and the circuit is optimized for phase noise. Next, the output buffers are added. The DC voltage at the output of the VCO may need to be adjusted, but a smooth PSS transient response should be achieved. Check a few points over the full tuning range to ensure the output swing is met. A good output buffer design will ensure that the output swing is good to go for the rest of the design. Tweak tank capacitance as needed to re-meet tuning range.
6. All devices are added, and now it is time to optimize the figure of merit by optimizing the phase noise. Run a PNOISE analysis and check the noise summary for the top contributing devices.
    a. At this point in the design, it may be necessary to replace the current mirror with a tail resistor if the current mirror is contributing significant noise.
    b. As the circuit is tweaked to lessen noise sources, periodically check the tuning range and band overlap and correct as necessary. Review the lectures on noise to best understand how to reduce the different noises.
        i. If the DC voltage at the output changes, the output buffers may need re-adjusting.
        ii. For this design, the band switches, varactor, and cross-coupled PMOS/NMOS pairs needed to be increased in size. The PMOS/NMOS pairs were increased until thermal noise limited size increase. The band overlap was at 70% and higher and so increasing the band switch sizes was do-able. The ideal fixed capacitance was steadily lowered as each device size was increased to offset introduced capacitance.
        iii. It may be necessary to meet the figure of merit specification by at least 1 dB as the final PSS sweep for this design had figures of merit 0.5 dB less than the figure of merit seen at the edges of each band.
7. After achieving the figure of merit, adjust the tank capacitance, varactor, and band switches as necessary to meet band overlap and tuning range.
8. Perform a fine sweep over the worst case band and plot its K_{VCO} which is just the derivative of the VCO frequency with respect to control voltage. There should be a peak.
    a. For this design, the worst case K_{VCO} was for the uppermost band. It may be worth the time for a full PSS sweep at this point to determine which band has the worst case (highest peaked) K_{VCO}.
    b. Adjust the varactor and bandswitch capacitors as necessary to lower K_{VCO}.
    c. It may be worth it to make minor adjustments to lower K_{VCO} and then re-adjust the tuning range as necessary rather than one big adjustment to get K_{VCO} in specification.
9. Check that the output swing is still met. If not, adjust the circuit as necessary. This design did not have to re-adjust for output swing as the DC voltage at the output was maintained at 1.416 V.
10. There is a trade off between phase noise (indirectly the figure of merit), the tuning range and band overlap, and K_{VCO}. Iterate over steps 6, 7, 8, and 9 until all specifications are met. It is possible that this is not possible, or easily achievable with the current number of bits. For this design, there was no wiggle room to lower K_{VCO} without losing band overlap or violating the figure of merit. A high Q value inductor will help with the issue of figure of merit. However, if K_{VCO} cannot be met, or any one specification cannot be met, then another bit must be added.
11. This design did not add another bit. It was determined that the K_{VCO} was satisfactory, due to time constraints. If another bit had been added, then the design would be iterated starting at the beginning of this methodology, but ignoring specific steps, such as using a current mirror or adding an output buffer. Additionally, the varactors and band switches would need to be redesigned to account for another bit and the fixed tank capacitance adjusted. Adding another bit doubles the simulation time as well.
12. Continue iteration and tweaking and adding bits as necessary until all specifications are met.

5. Schematics - Component Values

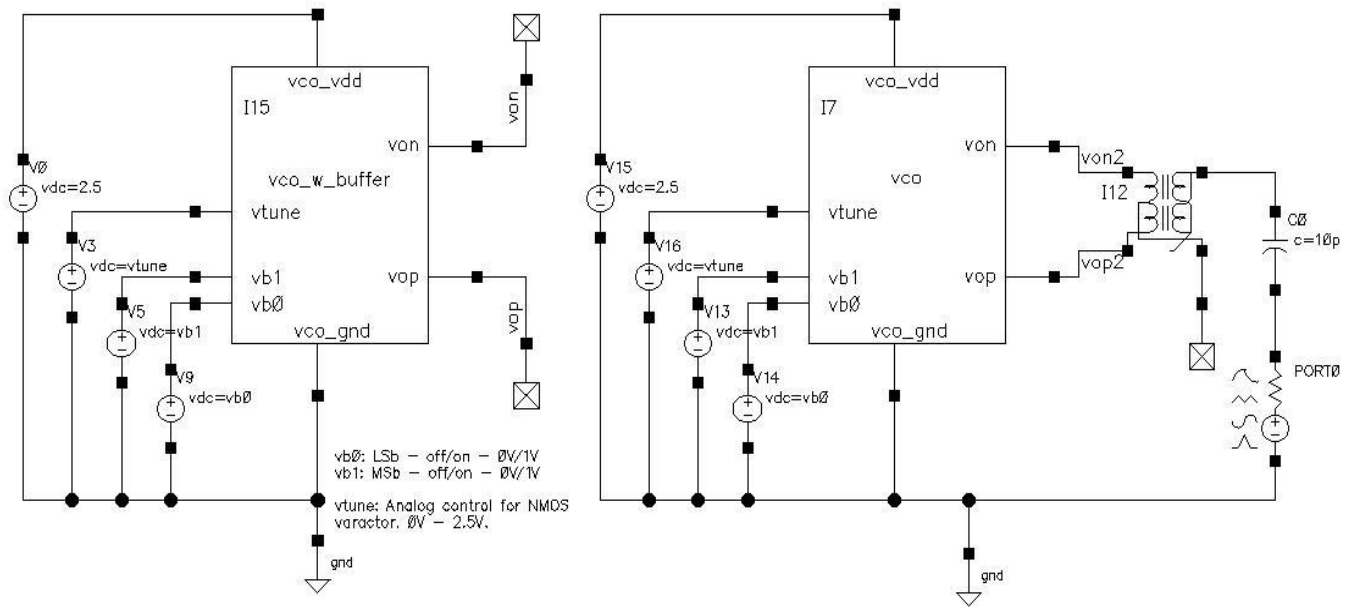


Figure 1: VCO testbench with component values. Left testbench used for PSS analysis and right testbench used for S-Parameter sweep.

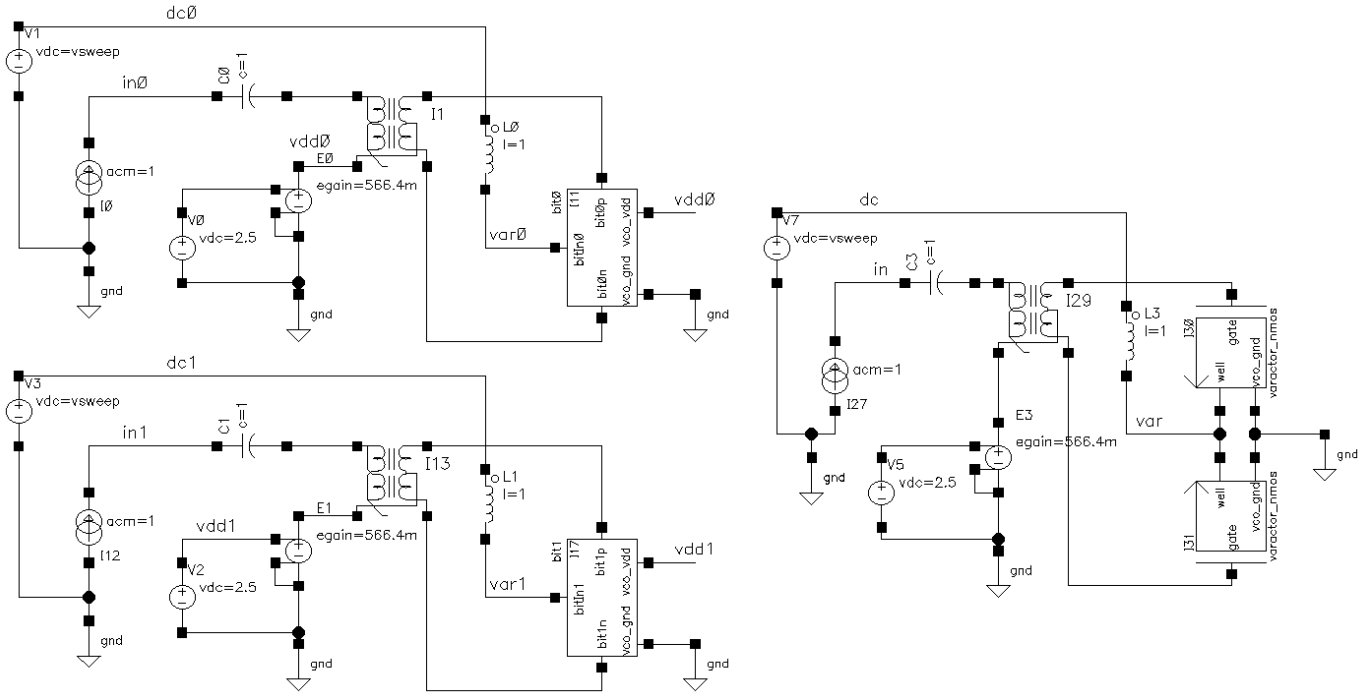
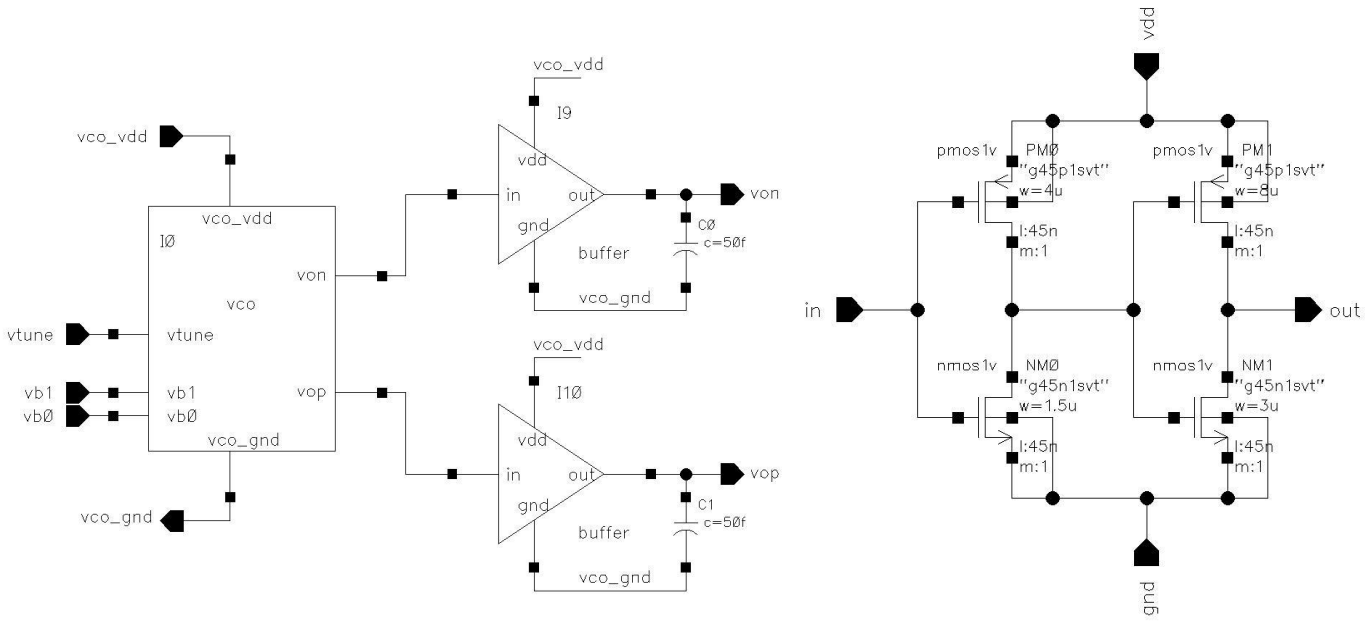


Figure 2: Varactor and bandswitch capacitor testbench with component values. The *egain* is set to achieve the same DC bias as the VCO circuit.



(a) (b)

Figure 3: Schematic with component values for both (a) the VCO with buffered output and 50 fF load and (b) the output buffer. The output buffer consists of a progressive inverter.

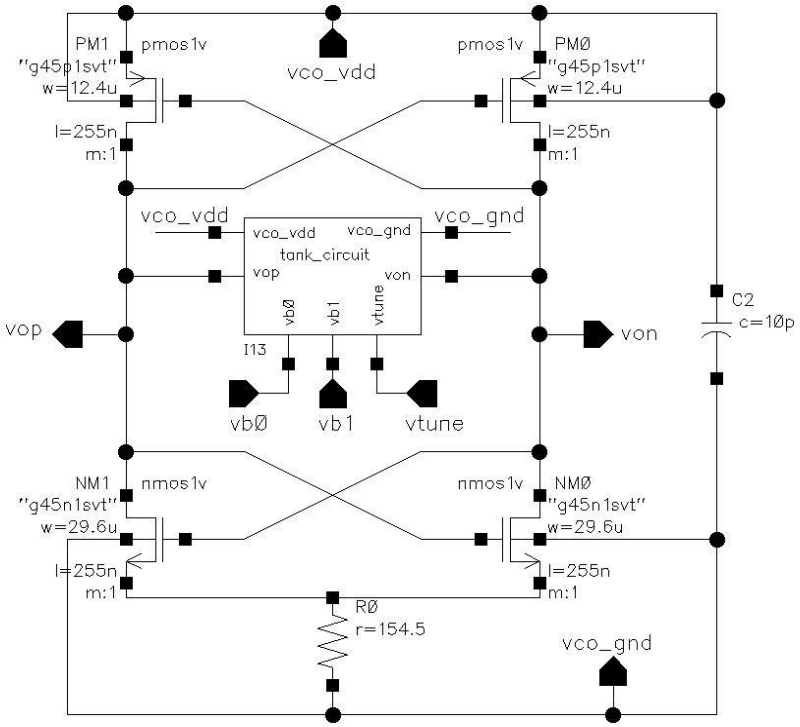


Figure 4: Schematic of the VCO at its component level, with the component values. The on-chip bypass capacitor is included at this level so that it would also be included in the S-Parameter testbench.

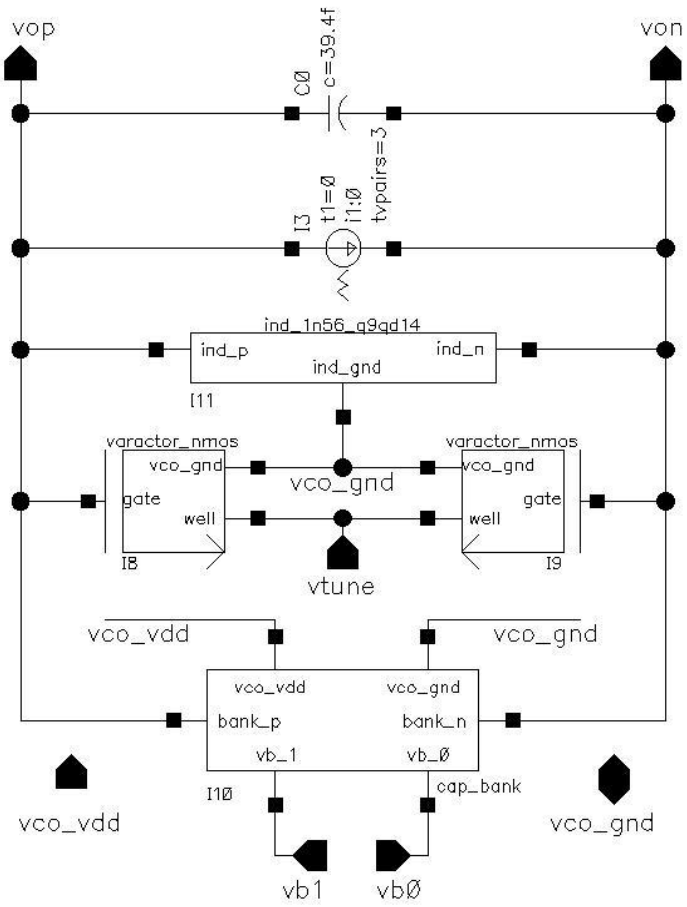
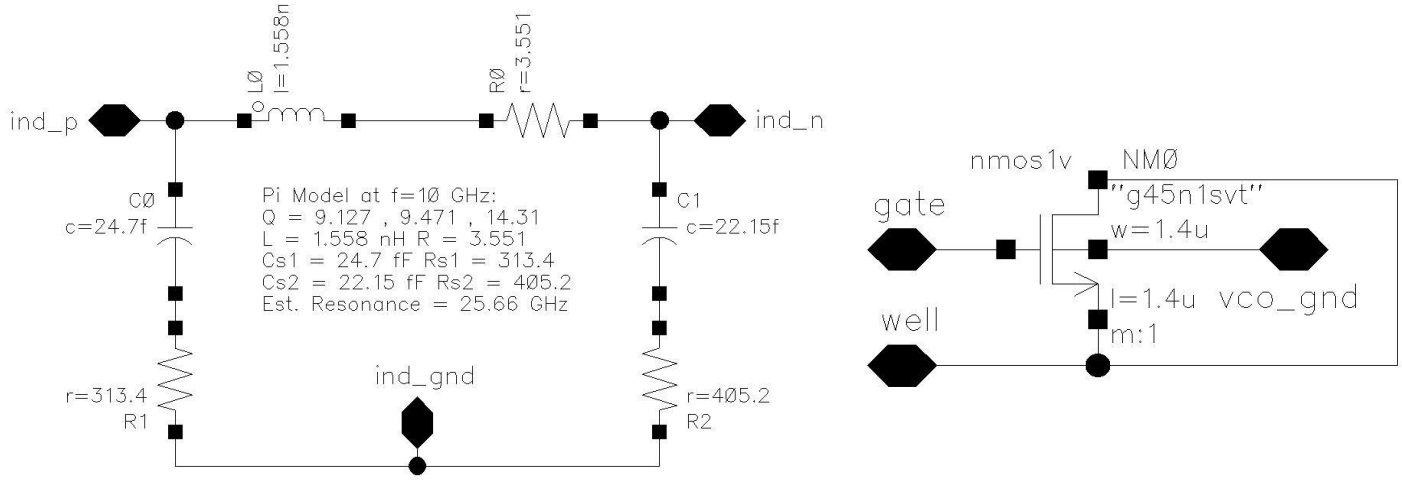


Figure 5: Tank circuit schematic with component values. The ideal current supply is used to kickstart the tank circuit by injecting 1 mA of current into the tank for 20 ps.



(a) (b)

Figure 6: Component values for both (a) the tanks ASITIC inductor and (b) the NMOS varactor. The relevant ASITIC Pi Model information can be found in the schematic in (a).

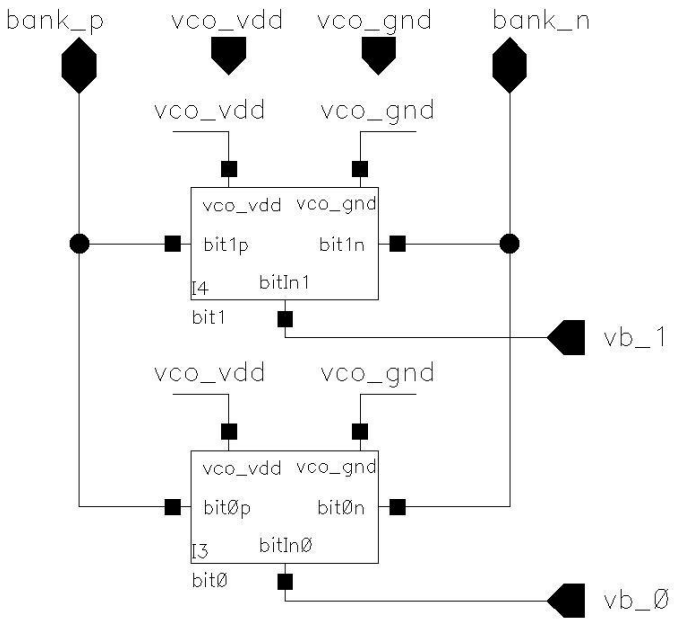
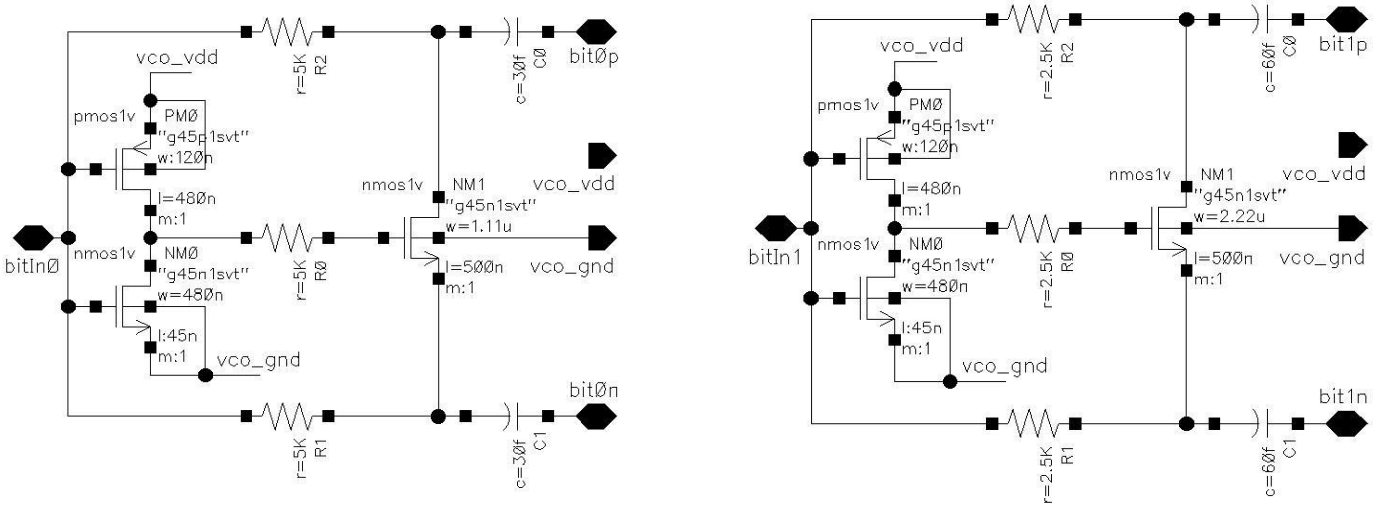


Figure 7: Capacitor bank schematic with component values. The capacitor bank has 2 bits (4 bands) and is controlled by the voltage signals *vb_0/vb0* and *vb_1/vb1* from the VCO schematic.



(a) (b)

Figure 8: Each bit in the capacitor bank is a differential bandswitch. The schematic with component values is shown for both (a) the LSb (bit 0) and the MSb (bit 1).

6. Performance Plots

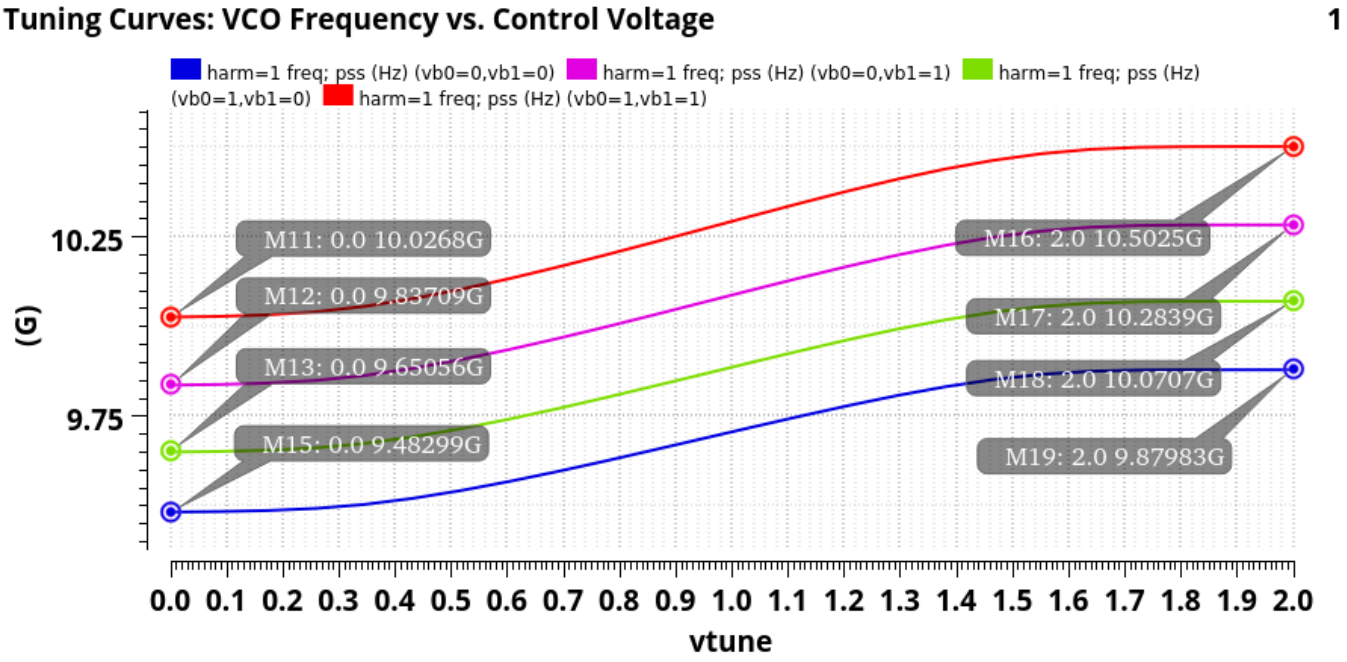


Figure 9: VCO Frequency versus control voltage, *vtune*. The band overlaps are calculated in section 1. This VCO design uses 2 bits, 4 bands. The frequency range is 9.483 GHz to 10.502 GHz. For this plot *vtune* consists of 25 data points. The calculation for this plot is given in section 1.

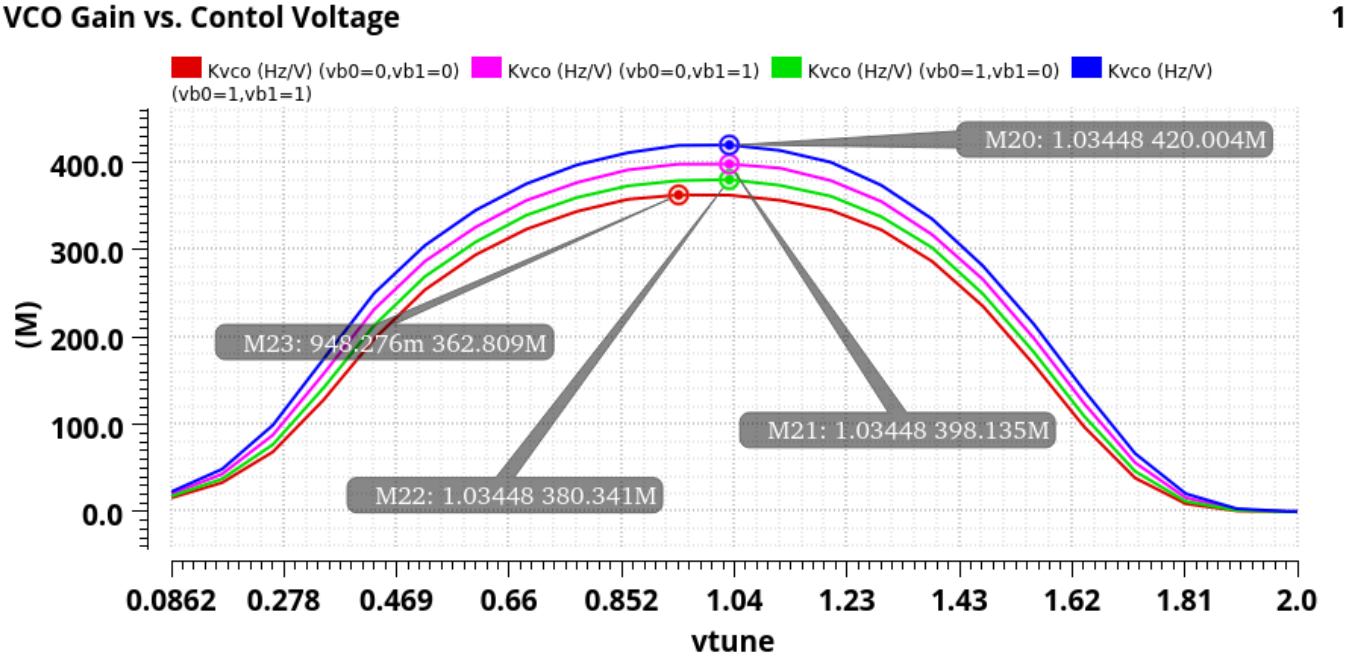


Figure 10: VCO gain (K_{VCO}) versus control voltage, *vtune*. The VCO gain is at best 362.809 MHz/V and at worst 420.004 MHz/V. For this plot *vtune* consists of 25 data points. The calculation for this plot is given in section 1.

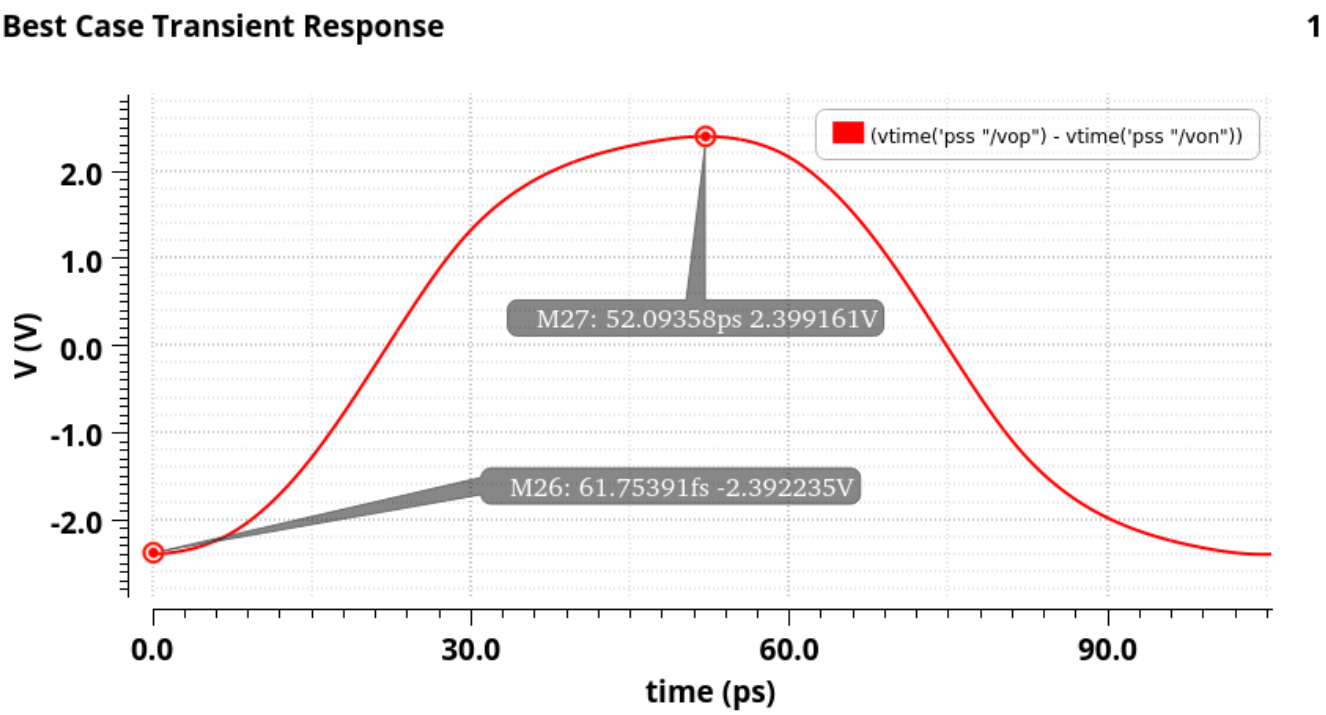


Figure 11: Transient response showing the best output swing of 4.79 Vppd. This occurs with the bias conditions, vb0 = 0 V, vb1 = 0 V, and vtune = 172.4 mV.

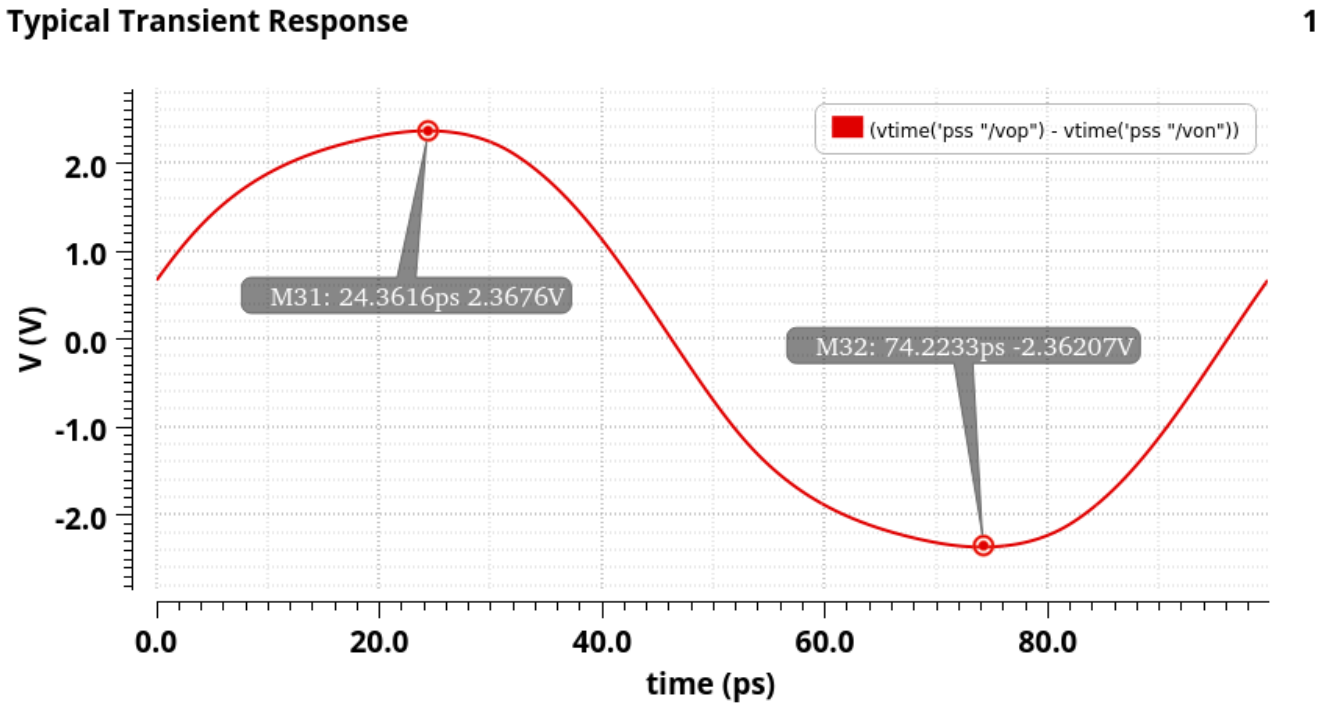


Figure 12: Transient response showing the typical output swing of 4.72 Vppd. This occurs with the bias conditions, vb0 = 1 V, vb1 = 1 V, and vtune = 86.21 mV. The typical response was selected by looking for the most common transient response.

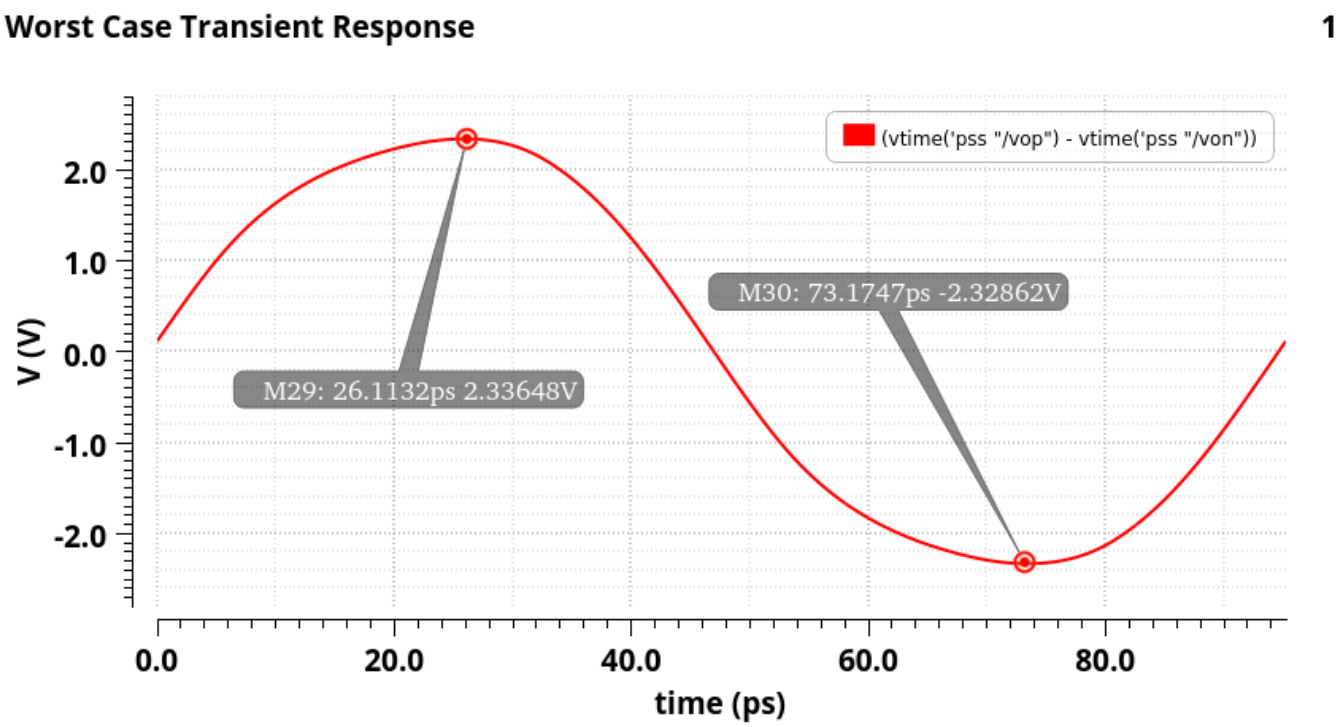


Figure 13: Transient response showing the worst output swing of 4.66 Vppd. This occurs with the bias conditions, vb0 = 1 V, vb1 = 1 V, and vtune = 2.414 V.

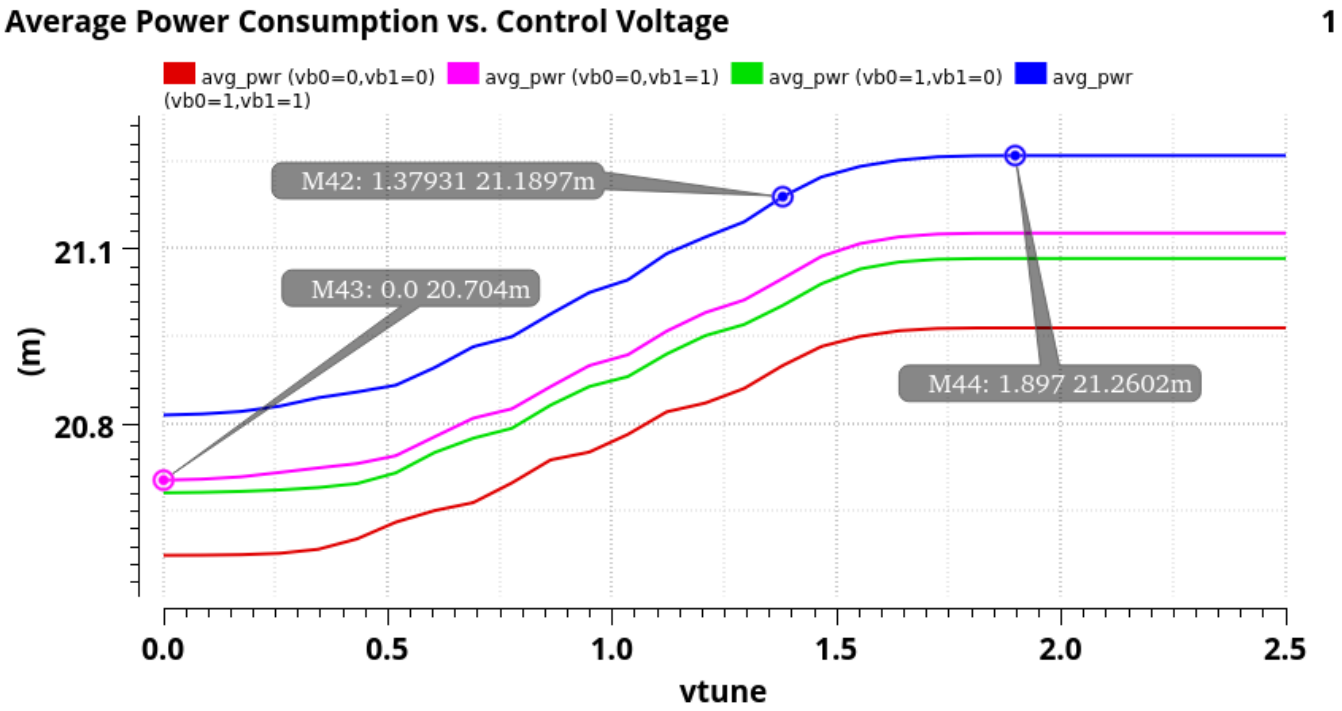


Figure 14: Average power consumption of the VCO for different control voltage configurations. The marked powers were used to calculate the best, typical, and worst case figures of merit. The calculation for average power is given in section 1.

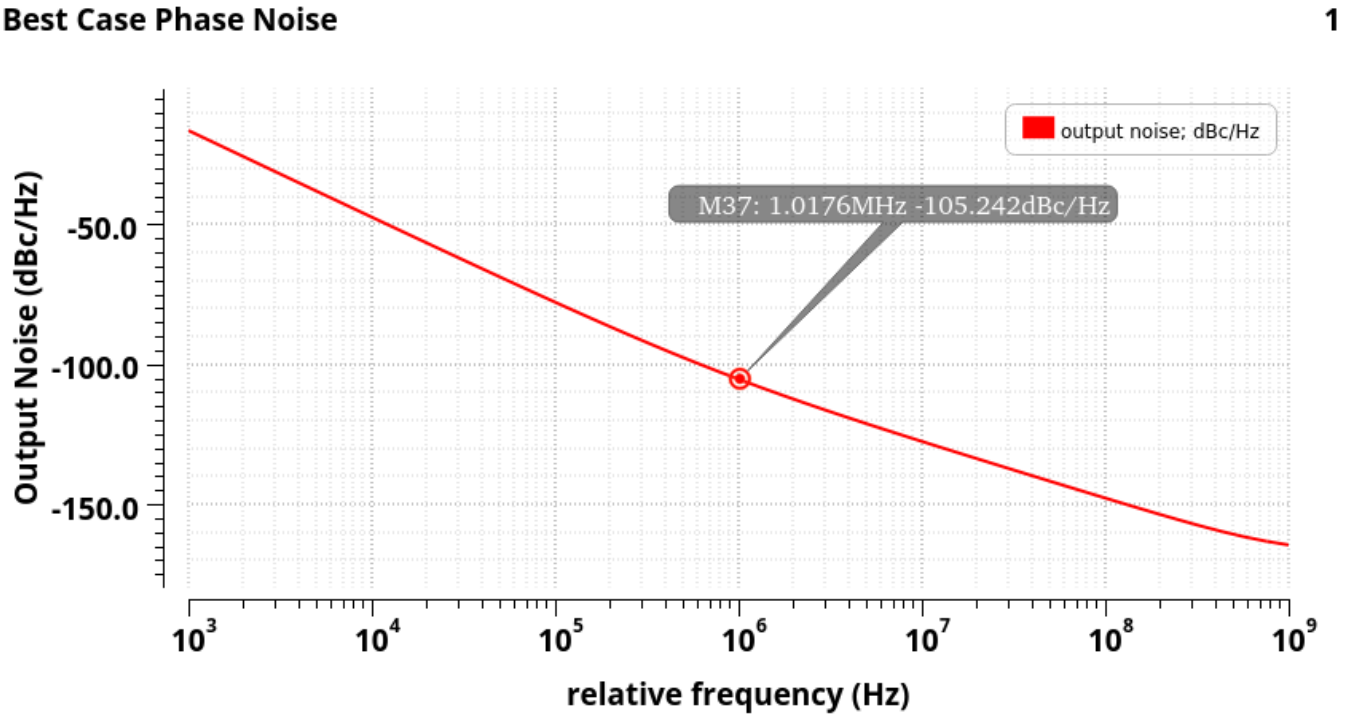


Figure 15: The best phase noise at 1 MHz relative offset to oscillator frequency happens when vb0 = 0 V, vb1 = 1 V, and vtune = 0 V.

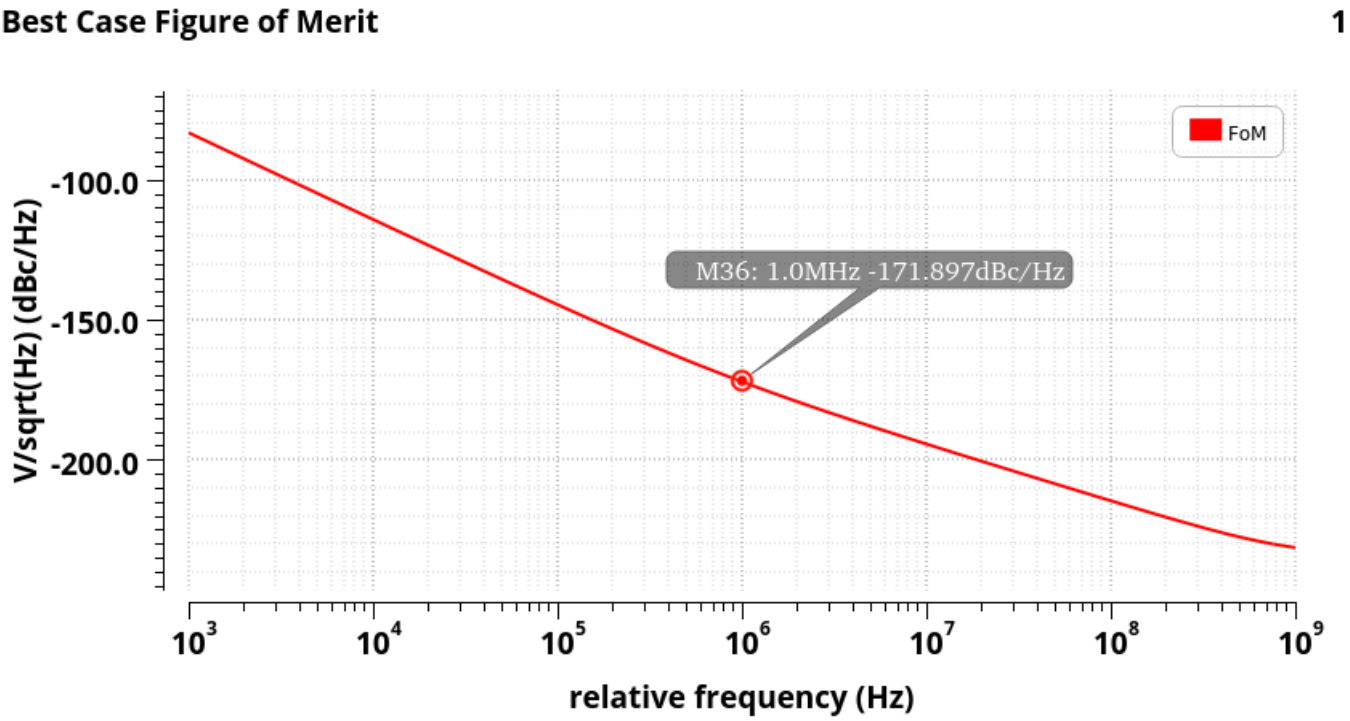


Figure 16: The best figure of merit at 1 MHz relative offset to oscillator frequency happens when vb0 = 0 V, vb1 = 1 V, and vtune = 0 V. The calculation for figure of merit is given in section 1.

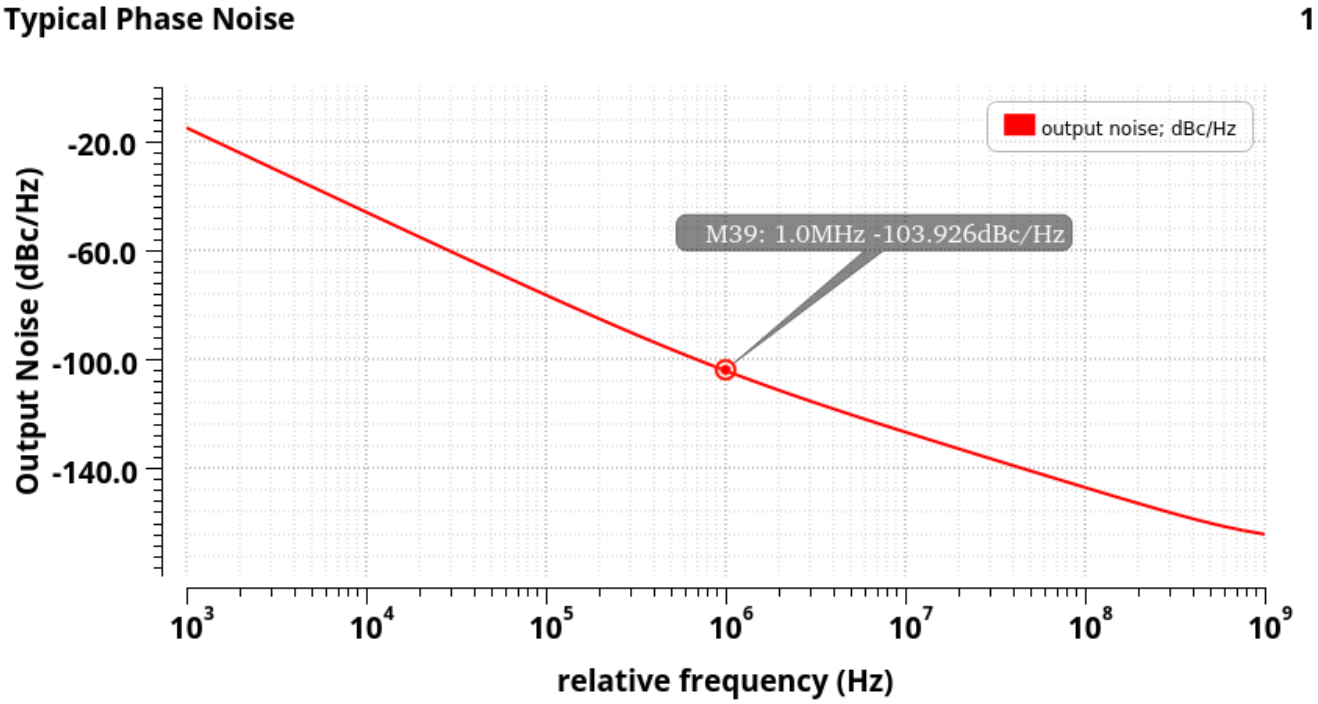


Figure 17: The typical phase noise at 1 MHz relative offset to oscillator frequency happens when vb0 = 1 V, vb1 = 1 V, and vtune = 1.897 V. The typical response was selected by looking for the most common phase noise at 1 MHz.

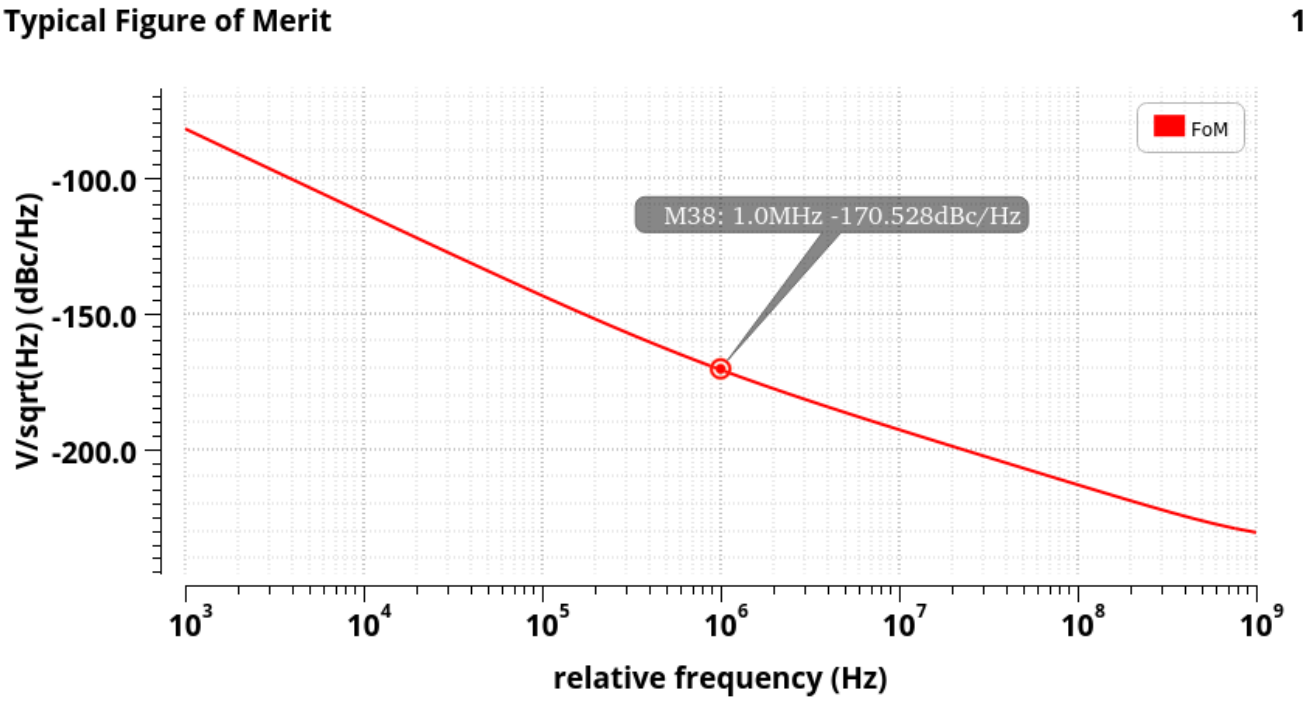


Figure 18: The typical figure of merit at 1 MHz relative offset to oscillator frequency happens when vb0 = 1 V, vb1 = 1 V, and vtune = 1.897 V. The calculation for figure of merit is given in section 1. The typical response was selected by looking for the most common figure of merit.

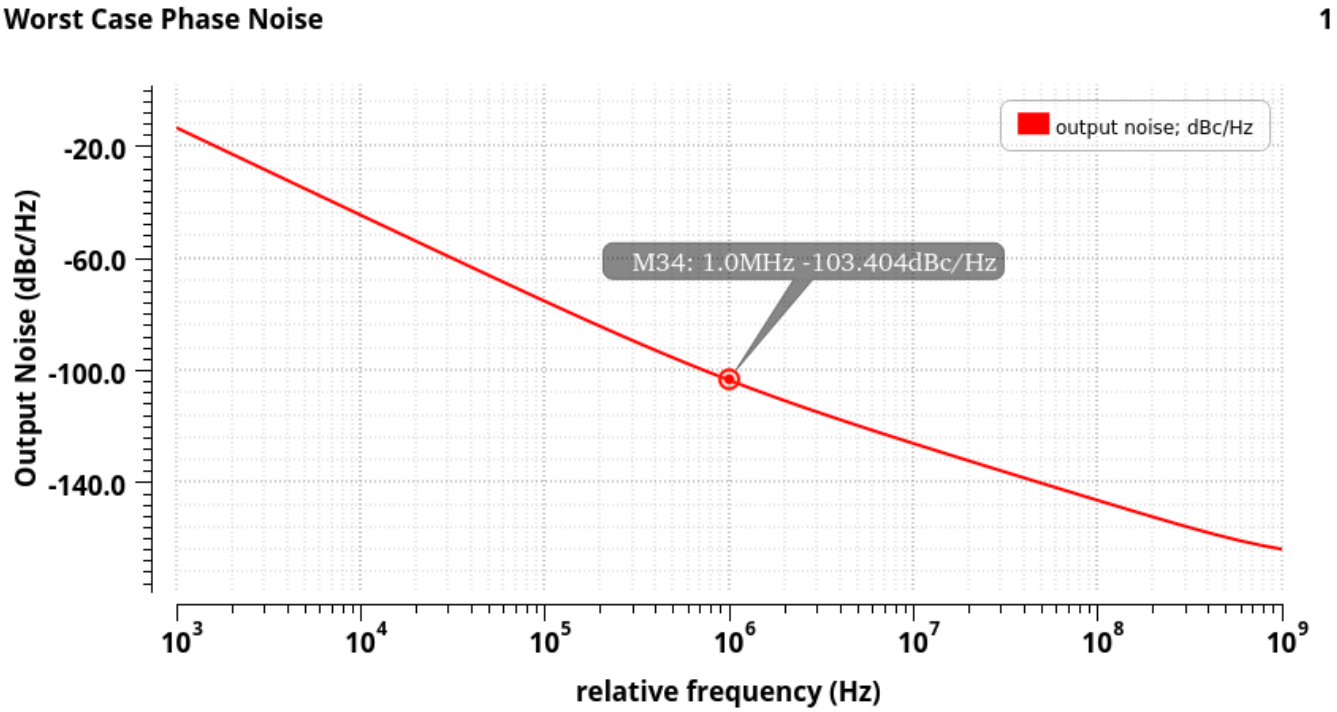


Figure 19: The worst phase noise at 1 MHz relative offset to oscillator frequency happens when vb0 = 1 V, vb1 = 1 V, and vtune = 1.37931 V.

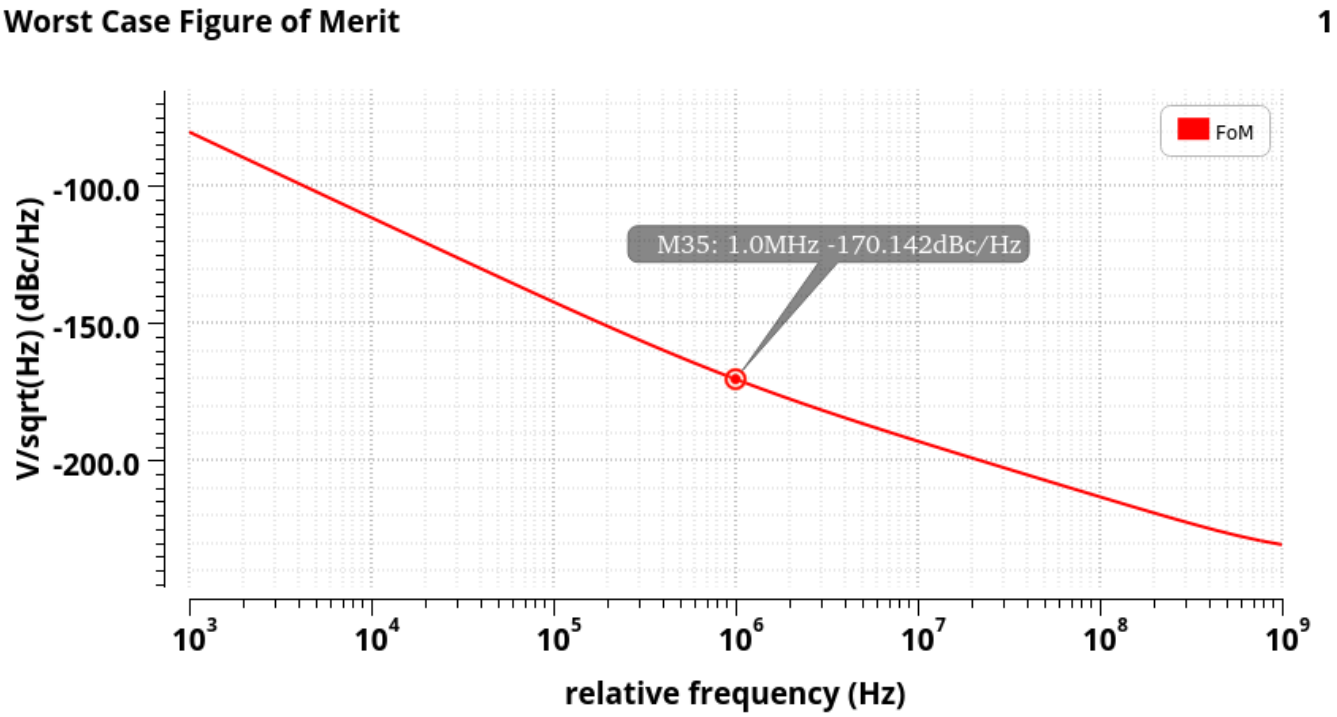
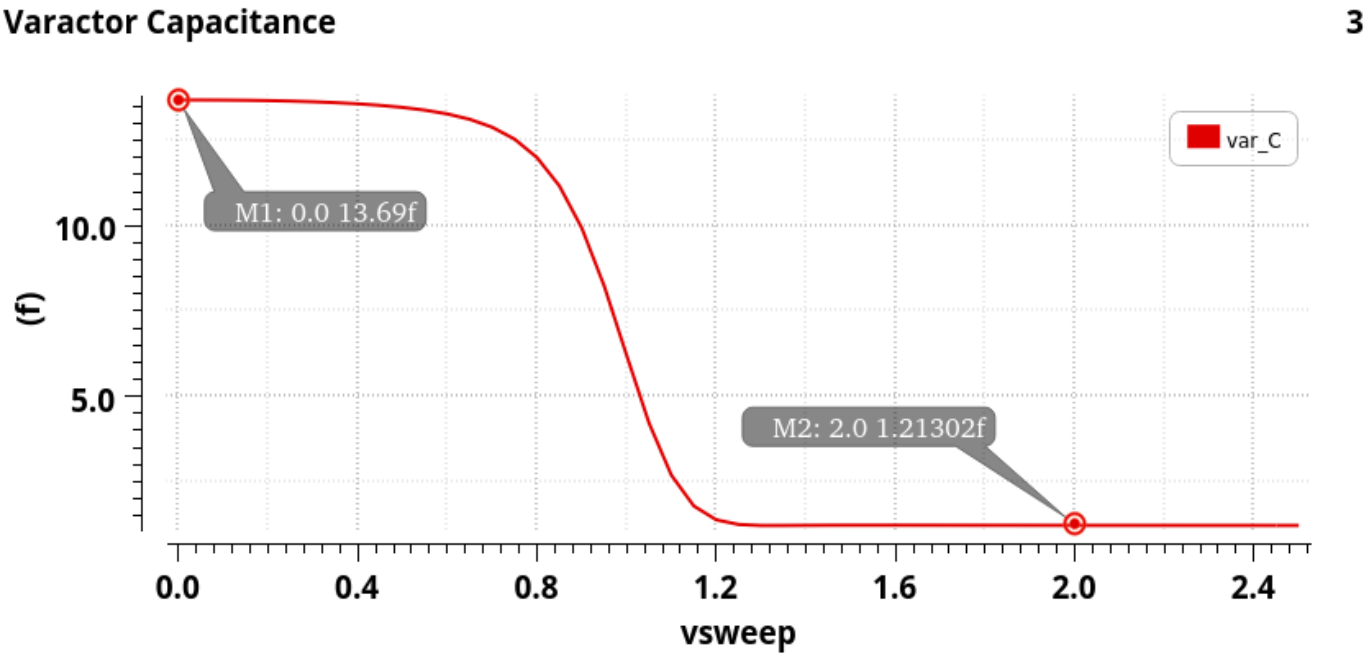
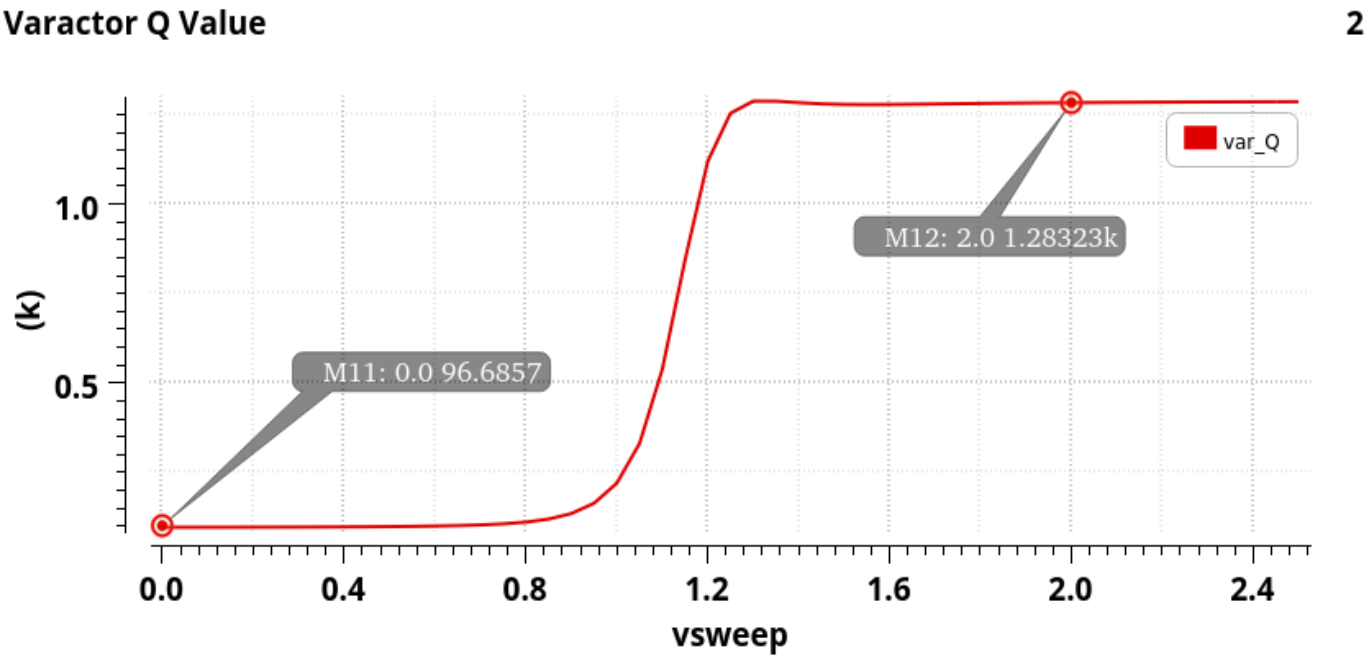


Figure 20: The worst figure of merit at 1 MHz relative offset to oscillator frequency happens when vb0 = 1 V, vb1 = 1 V, and vtune = 1.37931 V. The calculation for figure of merit is given in section 1.

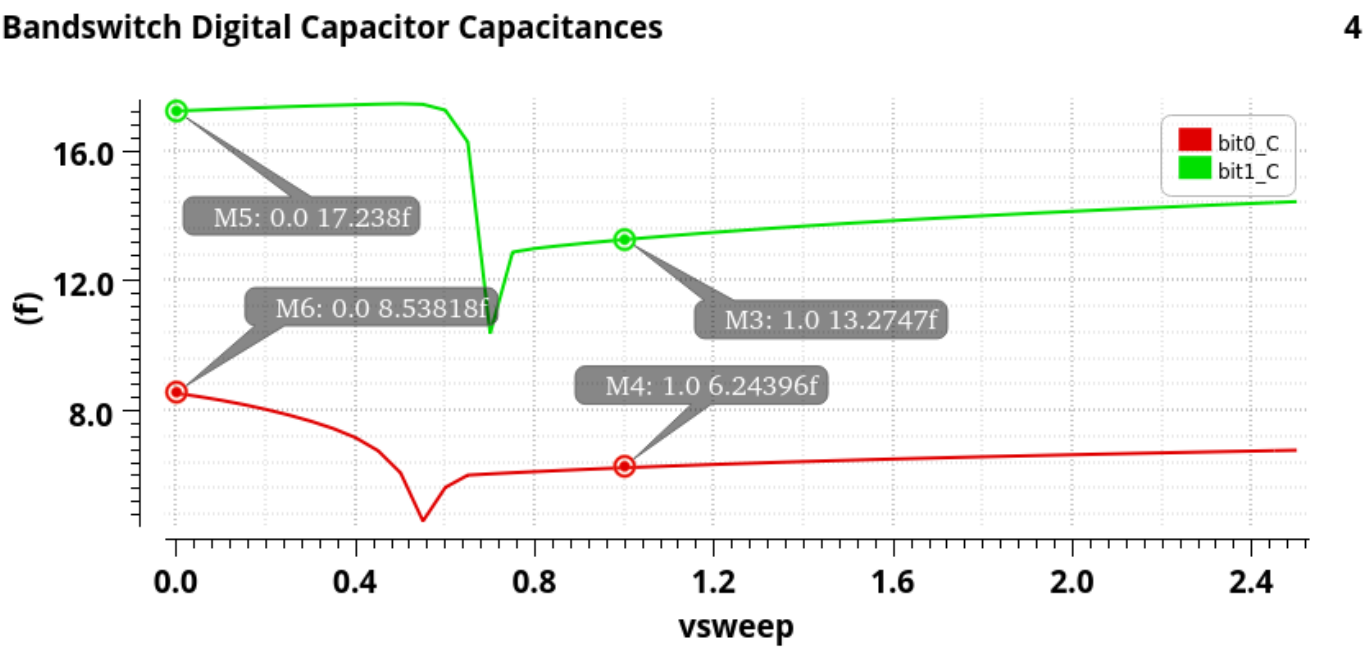


(a)

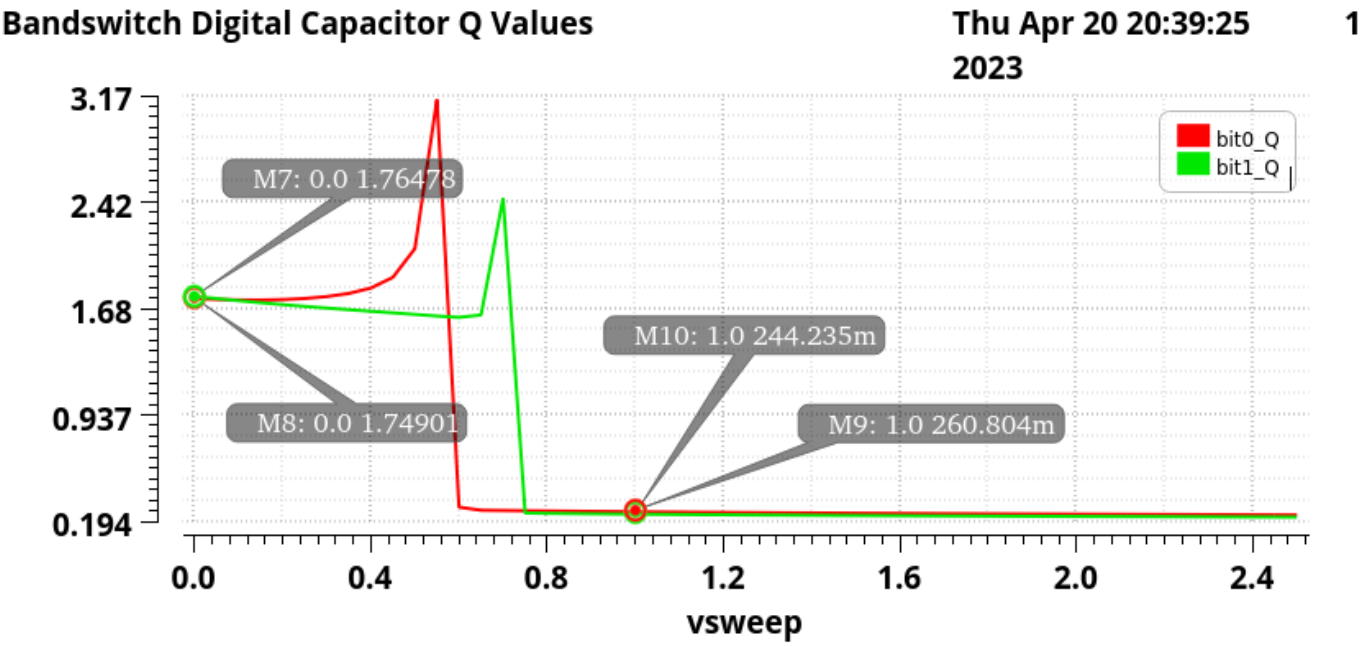


(b)

Figure 21: The (a) NMOS varactor capacitance value versus control voltage and the (b) NMOS varactor Q value versus control voltage. The control voltage is *vtune* in the VCO testbench and ranges from 0 V to 2 V. The capacitance is calculated with `((-1 * (imag(VF("/in"))**-1)) / (2 * pi) / 1e+10)` and the Q value is calculated with `(-1 * (imag(VF("/in")) / real(VF("/in"))))`. Where "/in" can be any of the four nets on the varactor testbench at the output of the AC current supply.



(a)



(b)

Figure 22: The (a) bit 0 and bit 1 NMOS differential bandswitch capacitance values versus control voltage and the (b) bit 0 and bit 1 NMOS differential bandswitch Q values versus control voltage. The control voltage is *vb0* and *vb1* for bits 0 and 1 respectively in the VCO testbench and ranges from 0 V to 2 V. The capacitance is calculated with `((-1 * (imag(VF("/in"))**-1)) / (2 * pi) / 1e+10)` and the Q value is calculated with `(-1 * (imag(VF("/in")) / real(VF("/in"))))`. Where "/in" can be any of the four nets on the varactor testbench at the output of the AC current supply.

7. Conclusion

During the course of the design, a few key interlocks were observed. The most common was the capacitance associated with adding and sizing devices. Device sizes directly influence phase noise, tuning range, and K_{VCO}. The more capacitance in the tank, the less pronounced the effect of adding additional capacitance on VCO frequency. Related to this observation was the size of the inductor. With too small of an inductor, as was the initial case, the large amount of capacitance needed to maintain 10 GHz VCO frequency led to not being able to meet the tuning range requirement with four bands and so the inductance was increased. Even still, there was fixed capacitance left in the final design and so a slightly larger inductor could have been chosen. If an additional bit was added, the fixed capacitance may not have been enough to account for the added band switch and so at that point, the inductor would have needed to decrease.

This design struggled to hit the figure of merit and so early in the design it would have been beneficial to attempt to achieve a higher Q inductor, though it is uncertain if a differential Q of greater than 15 would have been achievable for an inductance between 1.4 and 1.6 nH. However, the design would have benefited greatly with more wiggle room with the figure of merit, so that the other devices could be changed freely to achieve tuning range, band overlap and K_{VCO}.

The last point to discuss is the tradeoff between K_{VCO}, tuning range, and band overlap. Due to a time constraint and constrained human resources, K_{VCO} was decided to be left unmet. However, the path to achieve K_{VCO} is known and outlined in section 4. The solution is to increase the number of bits. With only two bits, K_{VCO} must violate specification in order to traverse 1 GHz. It is uncertain if the design would need more than three bits, but it would seem that K_{VCO} could be met with eight bands.

As noted in section 4, if another bit was added, then the circuit would need to be optimized again. The inductance may need to be adjusted to account for the capacitance added by the extra differential bandswitch. The added bit would be the most significant bit and should be large enough to not be the top noise contributor. However, with the tight tolerance on the figure of merit (0.1 dB), adding 10^-11 or 10^-12 V^2/Hz would likely have caused the figure of merit to not be met. This would be fixed by searching for a better inductor or by continuing to optimize device sizes. The added bands would allow the K_{VCO} to lessen while meeting tuning range and band overlap. The methodology from section 4 would be followed and the tuning range, band overlap, the figure of merit, and K_{VCO} would be iterated on until met.

One issue that may arise with adding another bit, is that some devices would need to be sized down. This would contribute to flicker noise and worsen the figure of merit. If there was not sufficient wiggle room, and a better inductor could not be found, then the inductor value itself may be lowered. This would mean more capacitance in the tank and a diminished affect on VCO frequency from added capacitance. This would allow for larger devices to eliminate noise while keeping K_{VCO} down.

References

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Appendix A Schematics - DC Operating Point

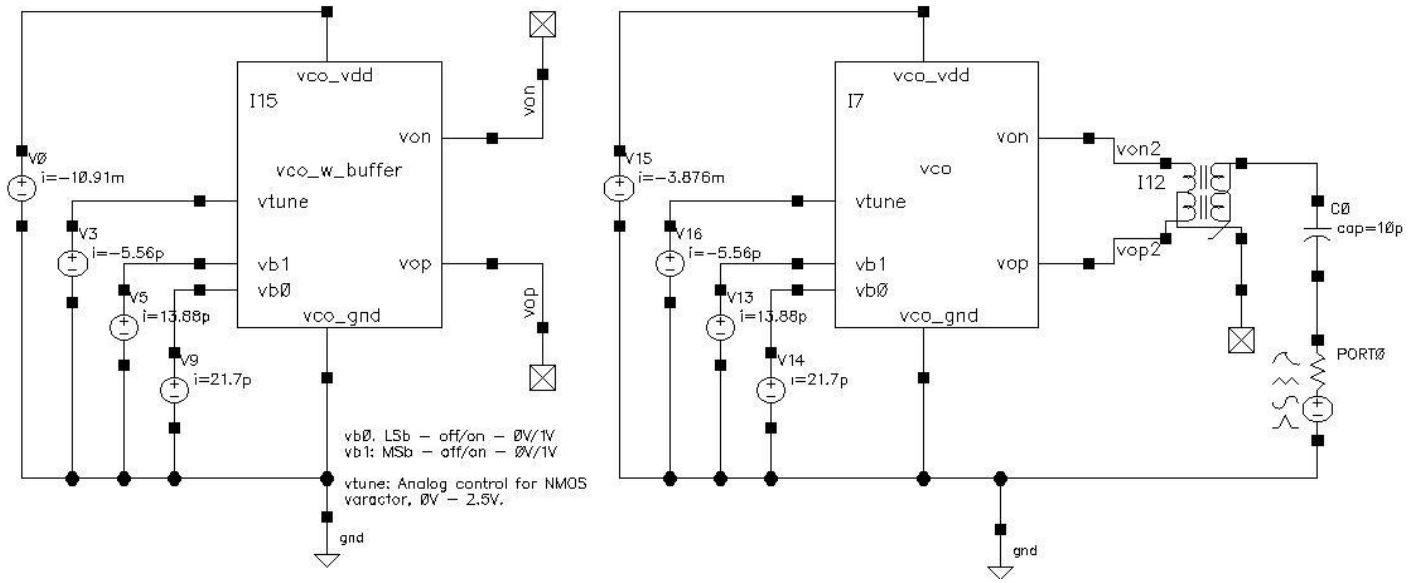


Figure 23: VCO testbench with DC operating point annotated. Left testbench used for PSS analysis and right testbench used for S-Parameter sweep. Operating point is, *vb0* = *vb1* = 1 V, and *vtune* = 1.4 V.

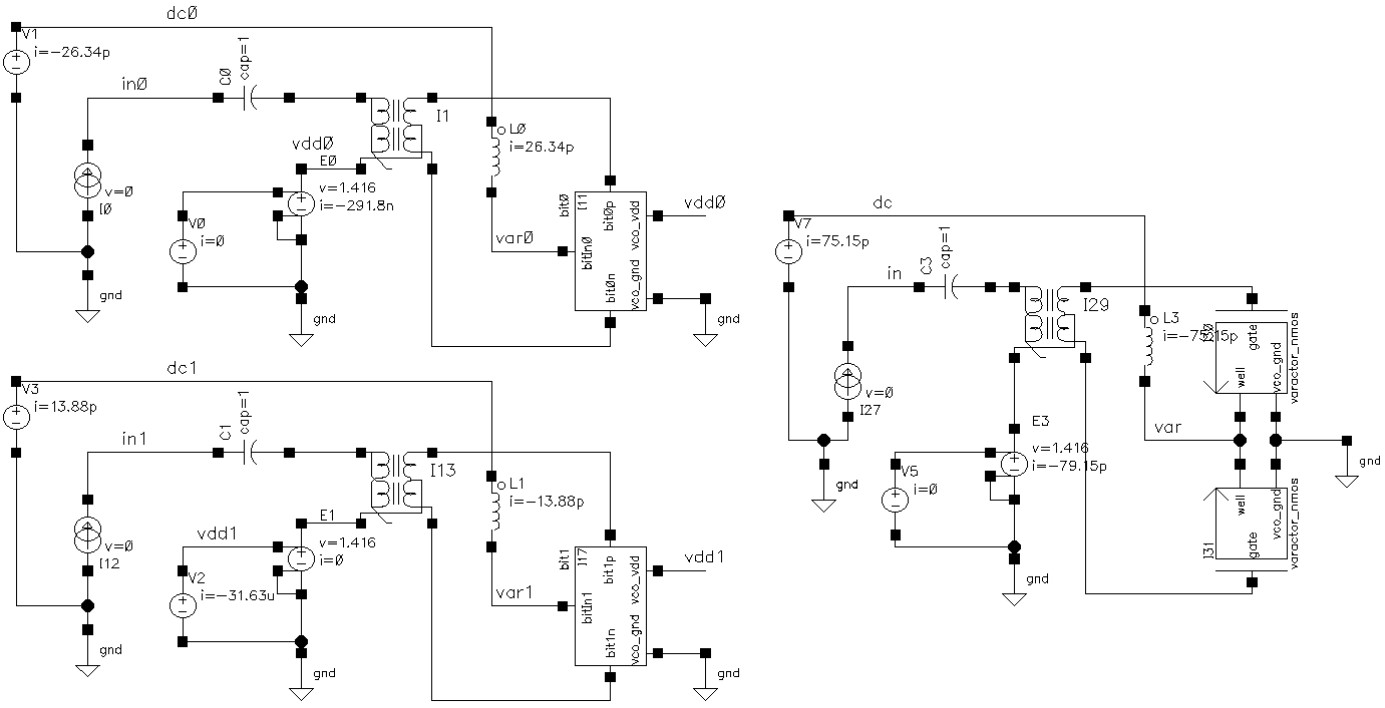
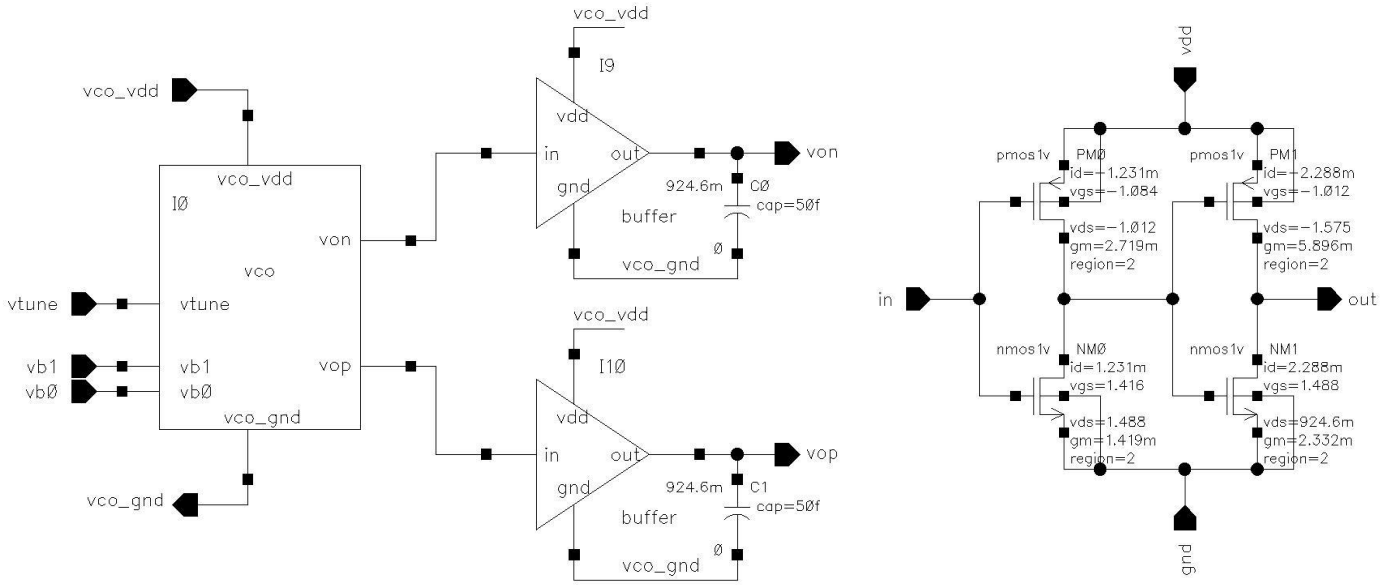


Figure 24: Varactor and bandswitch capacitor testbench with DC operating point annotated. The *egain* is set to achieve the same DC bias as the VCO circuit. The DC operating point is set with *vsweep* = 1 V.



(a) (b)

Figure 25: Schematic with annotated DC operating point for both (a) the VCO with buffered output and 50 fF load and (b) the output buffer. The output buffer consists of a progressive inverter. There is not much displayed for (a) with the DC operating point due to the symbol not being set up to do so. Operating point is, *vb0* = *vb1* = 1 V, and *vtune* = 1.4 V.

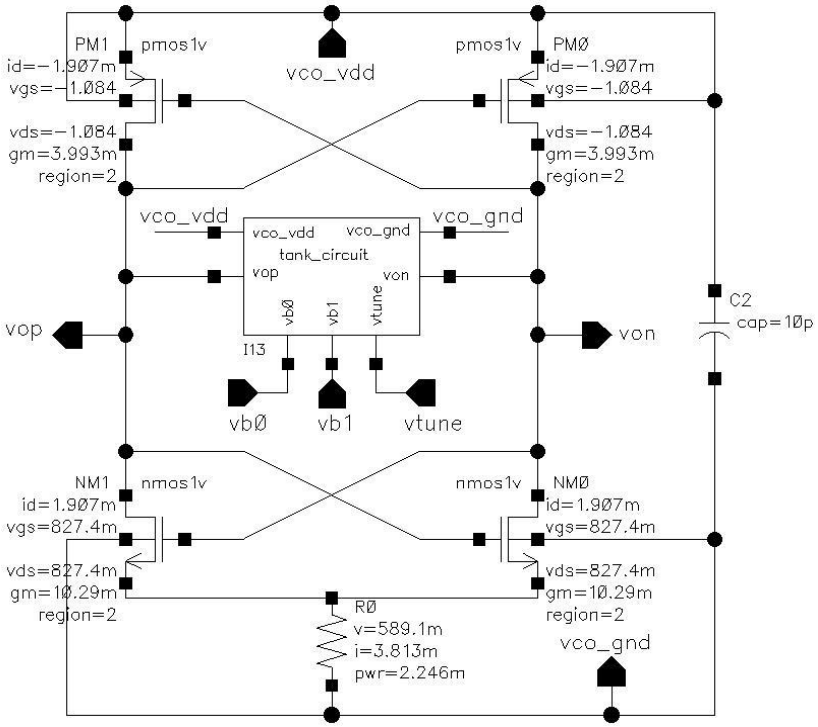


Figure 26: Schematic of the VCO at its component level, with the DC operating point annotated. The on-chip bypass capacitor is included at this level so that it would also be included in the S-Parameter testbench. Operating point is, *vb0* = *vb1* = 1 V, and *vtune* = 1.4 V.

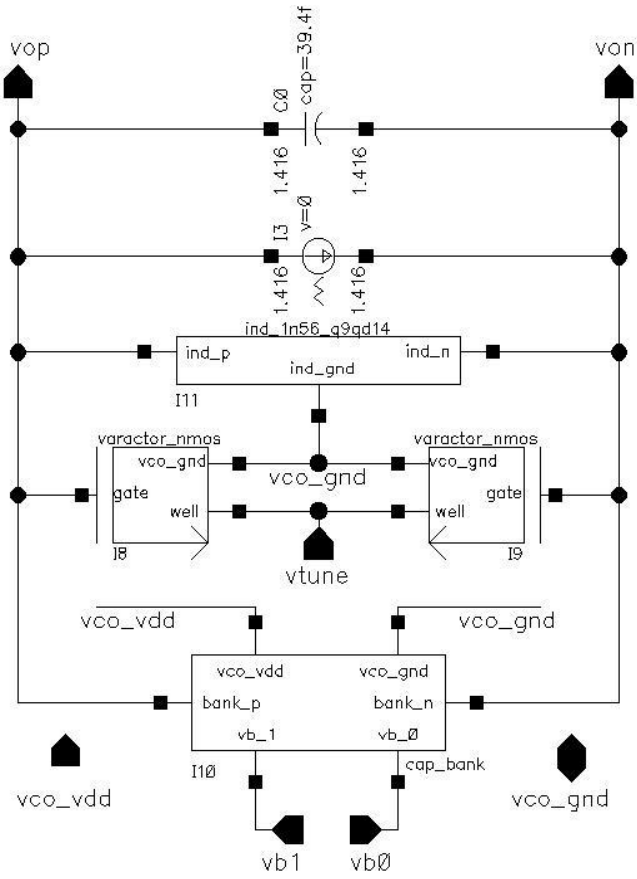
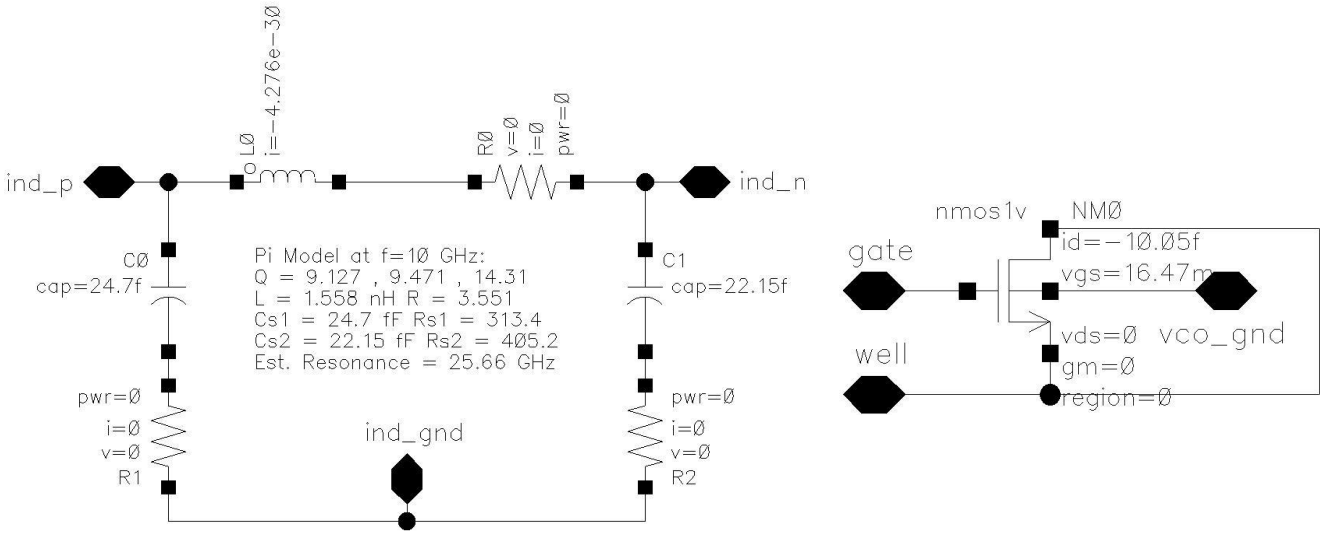


Figure 27: Tank circuit schematic with annotated DC operating point. The ideal current supply is used to kickstart the tank circuit by injecting 1 mA of current into the tank for 20 ps. Operating point is, *vb0* = *vb1* = 1 V, and *vtune* = 1.4 V.



(a) (b)

Figure 28: Annotated DC operating point for both (a) the tanks ASITIC inductor and (b) the NMOS varactor. The relevant ASITIC Pi Model information can be found on the schematic in (a).

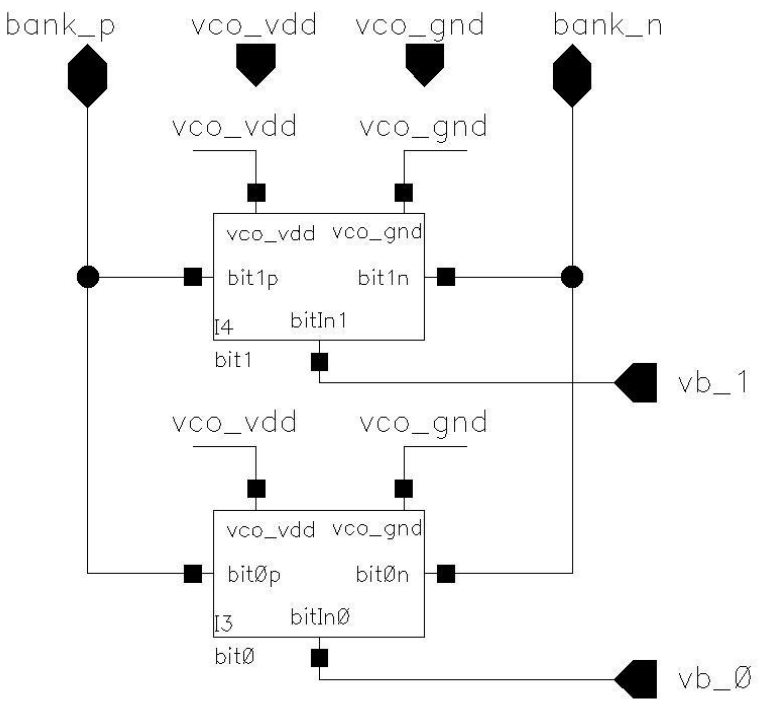
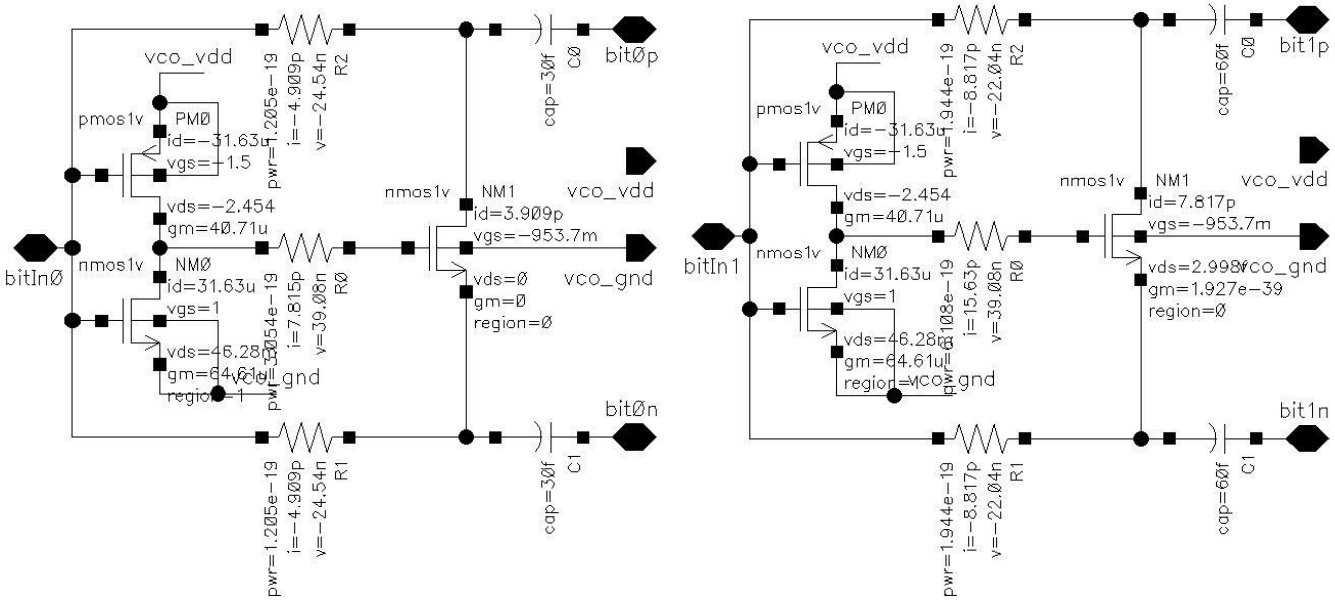


Figure 29: Capacitor bank schematic with annotated DC operating point. Due to the setup of the symbols, there are no values displayed. The capacitor bank has 2 bits (4 bands) and is controlled by the voltage signals *vb_0/vb0* and *vb_1/vb1* from the VCO schematic. Operating point is, *vb0* = *vb1* = 1 V, and *vtune* = 1.4 V.



(a) (b)

Figure 30: Each bit in the capacitor bank is a differential bandswitch. The schematic with component values is shown for both (a) the LSb (bit 0) and the MSb (bit 1). Operating point is, *vb0* = *vb1* = 1 V, and *vtune* = 1.4 V.