Project 1: Complementary Metal Oxide Semiconductor Low Noise Amplifier

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William T. Jarratt pledges that all work contained within represents his own work and the work of nobody else.

Contents

Abstract

This document details the design of a cascoded common source low noise amplifier (LNA) with inductive degeneration. The on chip inductors are all modeled with ASITIC PI models. The resulting LNA design achieves a peak gain of 15 dB at 9.76 GHz, maintains a noise figure below 1.71 dB across 9.5 GHz to 10.5 GHz, consumes less than 5 mW of power, and achieves a 1 dB compression and IP3 just above -16 dBm and -3 dBm respectively. This document walks through the choices made throughout the design process, shows resulting simulations and circuit typologies, and summarizes the performance of the LNA.

1 Specification Table

Table 1 shows the requirements for the low noise amplifier, along with the results from the design described in this article. Plots or schematics showing the relevant result are also given. Any specifications that require additional explanation are noted with superscript numbers and the explanation is given below. Specifications not met have their row highlighted red.

Specifications and Results			
Metric	**Specification**	**Result**	**Shown by**
Center Frequency[1]	10 GHz	9.76 GHz	Fig. 11
3 dB Bandwidth (BW)[2]	10% fractional	30.5%	Fig. 11
Noise Figure	$<$ 2.7 dB (full BW)	$<$ 1.71 dB	Fig. 14
Power Consumption	$<$ 5 mW	4.989 mW	Fig. 20
Gain, $\lvert S_{21}\rvert$[3]	$>$ 15 dB peak in BW	15.0025 dB peak	Fig. 11
Input Match, $\lvert S_{11}\rvert$	$<$ -10 dB (full BW)	$<$ -12.573 dB	Fig. 15
Output Match, $\lvert S_{22}\rvert$	$<$ -10 dB (full BW)	$<$ -10.002 dB	Fig. 15
Input Referred IP3	$>$ -3 dBm	-2.98 dBm	Fig. 19
1 dB Compression Point	$>$ -13 dBm	-15.96 dBm	Fig. 18
K Stability	$>$ 1 DC to Daylight	$>$ 1.06	Fig. 16
B Stability	$>$ 0 DC to Daylight	$>$ 112 n	Fig. 16

Table 1: Specifications for low noise amplifier along with the results of the design.

1. The center frequency, f_c, is given as the frequency at which $|S_{21}|$ peaks. An alternative definition is the average frequency between the upper and lower 3 dB cutoff. From Fig. 11, it is shown that the 3 dB bandwidth (BW) is from 8.52 GHz to 11.57 GHz. This would make the average frequency, f_{ave} equal to 10.05 GHz.

2. The max $|S_{21}|$ is 15.0025 dB, meaning the 3 dB requirement is to be above 12.0025 dB between 9.5 GHz and 10.5 GHz. This is shown as achieved in Fig. 11. The fractional BW is calculated as:

$$\begin{aligned} BW_{frac} &= \frac{f_{max} - f_{min}}{f_{ave}} 100\%, \\ &= \frac{f_{max} - f_{min}}{f_c} 100\%, \\ &= \frac{11.57 \text{ GHz} - 8.52 \text{ GHz}}{10 \text{ GHz}} 100\%, \\ &= 30.5\%. \end{aligned} \tag{1}$$

   Alternatively, f_{ave} could be taken as 10.05 GHz and BW_{frac} would be 30.35%.

3. This specification was clarified on the class forum (link). The $|S_{21}|$ specification can be met at any point in the required 3 dB BW. The 3 dB BW is 9.5 GHz to 10.5 GHz.

2 Design Overview

The low noise amplifier (LNA) design used in this document is based on the recipe detailed in [1, 2, 3] for a cascoded common source amplifier with inductive degeneration. Current mode biasing is achieved by current mirror and an ideal current source. The recipe mentions sweeping the current for a single NMOS current mirror, but it was recommended to start with a cascoded current mirror. The design begins with ideal components, which are replaced with less ideal components as the design progresses.

The first circuit is shown in Fig. 1. Fig. 12 and Fig. 13 show the current sweep for a finger size of 5 and finger width of 1.52 μm. All gate lengths are 100 nm. It was noted that as gate length decreased G_{max} would peak at higher values and NF_{min} would decrease. Thus the smallest gate length allowed of 100 nm was chosen. The number of fingers and geometry were chosen so that the optimum NF_{min} and G_{max} would be less than 1 mA. This was decided with the power consumption limit in mind. The gate width of 1.52 μm is an artifact from a iteration before. However, the device sizes had to be large enough to avoid flicker noise. The reference current was chosen to be 595 uA, this was thought to give a good buffer to the 5 mW power limit, while also giving a large G_{max} and very low NF_{min}.

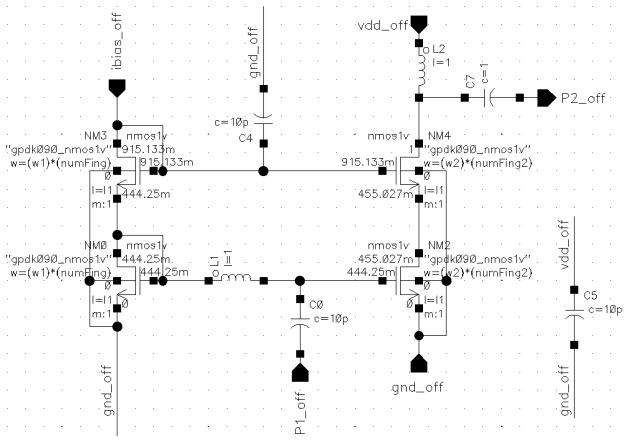


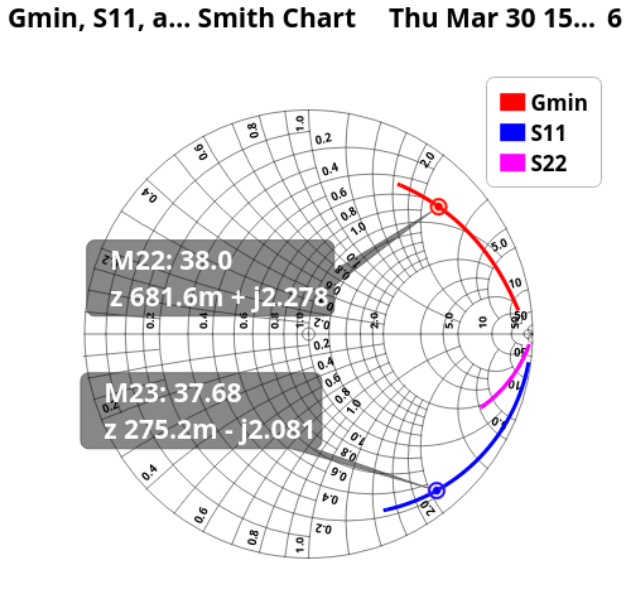
Figure 1: Initial LNA circuit, step 2 of recipe from [2].

The next step of the recipe was to replace inductor L1 with a resistive choke. An ideal resistor was used. It was cited in class that 1K to 10 KΩ were usual values, but 10 KΩ increased NF_{min} from 300 mdB to about 1 dB, and thus a higher resistance was chosen, 20 KΩ. This did not have an adverse affect on G_{max}. From previous iterations, it was clear that G_{max} would become an issue later and so care was taken to keep G_{max} as large as possible.

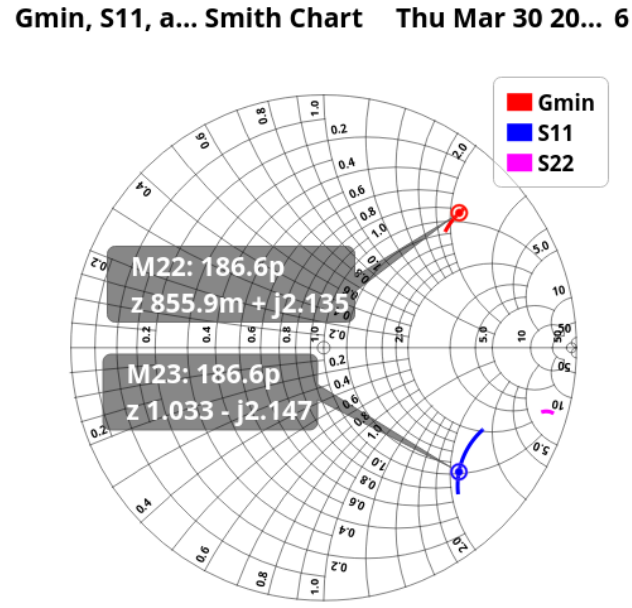
Next, the number of fingers for NM2 and NM4 were swept to move G_{max} close to the 50 Ω circle. This was overshot due to anticipated inward movement introduced by a non-ideal source and gate inductor. The number of fingers chosen was 38 and is marked on the smith chart in Fig. 2a.

In step 5 the source inductor is added to bring S_{11} towards the 50 Ω circle. Note that S_{11} is farther out than Γ_{opt} in Fig. 2a. The affect on Γ_{opt} is less than S_{11}. The source inductor has a Q associated with it and from previous iterations it is known that Q values at 15 and above are achievable. A high Q is important for the source inductor because a lower Q or larger source inductor resistance will lower G_{max} due to degeneration. The source inductance already lowers gain, but is needed for linearity. With a Q of 15, L_S was swept and the value chosen was about 170 pH, though later in the design process the value is adjusted to 186.6 pH to meet IP3. The L_S sweep and value at 186.6 pH is shown in Fig. 2a.

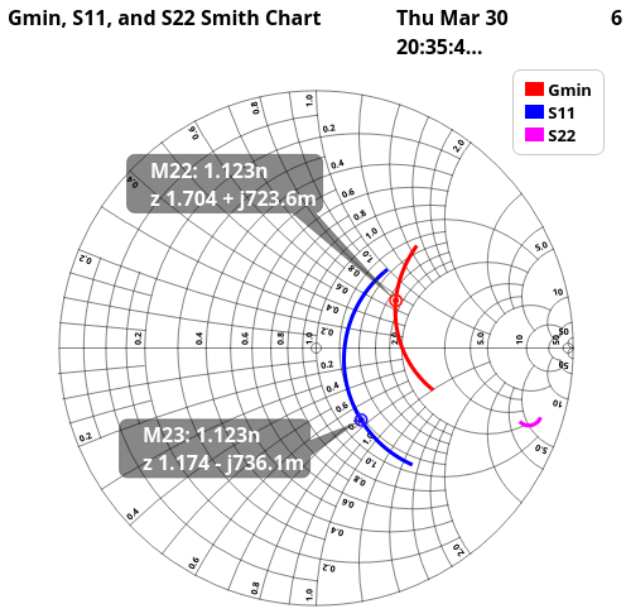
Next, the gate inductor is added and L_G is swept to bring both S_{11} and Γ_{opt} to the center of the Smith chart. This is step 6 in [2]. A Q value of 10 was chosen initially based on what had been seen in previous iterations for expected values of L_G. The Q value is important as it determines the deviation between S_{11} and Γ_{opt}. The sweep of L_G is shown in Fig. 2c. Initially, the value was chosen close to 1.75 nH, which would put S_{11} and Γ_{opt} both near the center. Ultimately, due to the affects of adding L_D and C_1, L_G was lowered to 1.123 nH. This is marked in Fig. 2c. Although S_{12} was less than -10 dB across bandwidth the LNA was still bilateral.



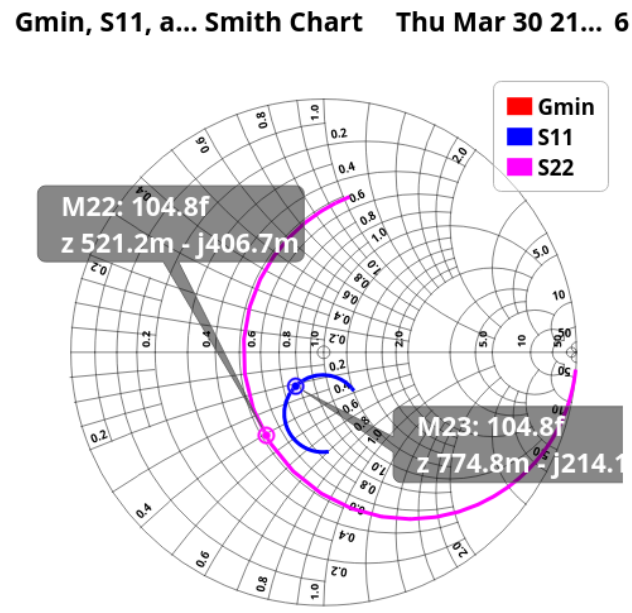
(a) Moving Γ_{opt} to 50 Ω circle, step 4 of recipe from [2].



(b) Moving S_{11} to the 50 Ω circle, step 5 of recipe from [2].



(c) Step 6 of recipe from [2]. Note that 1.75 nH was required to reach the center. Though it is known that 1.123 nH was the final value of L_G.



(d) Attempting to place S_{11} and S_{22} in center of Smith chart. The sweep shown is of C_1.

Figure 2: Progression of S_{11}, S_{22}, and Γ_{opt} while adding inductors.

From previous iterations, it was known that NF was less of an issue than gain and so it was decided to focus on S_{11} matching over NF matching. Also note that S_{11} could be closer to the center if L_S is decreases, this was true for this design iteration, but in the end L_S must be higher for linearity.

The next step, step 7 and 8, required matching the output with a drain inductor and two capacitors, however only one series capacitor was needed. Adding the output match affected the input match and thus L_G and L_S were changed with the output match to maintain both the input and output match. First S_{22} was swept out to the 50 Ω circle and then brought into the center with an ideal inductor. The drain inductance inductance ended up being 1.222 nH and series capacitor replaced the 1 F capacitor with a 104.84 fF capacitor. The capacitor sweep is shown in Fig. 2d. The initially chosen values of L_G and C_1 were chosen to put S_{22} and S_{11} close to the Smith chart center, however the values shown in the plot also account for the parasitics that come with the ASITIC inductors later in the design.

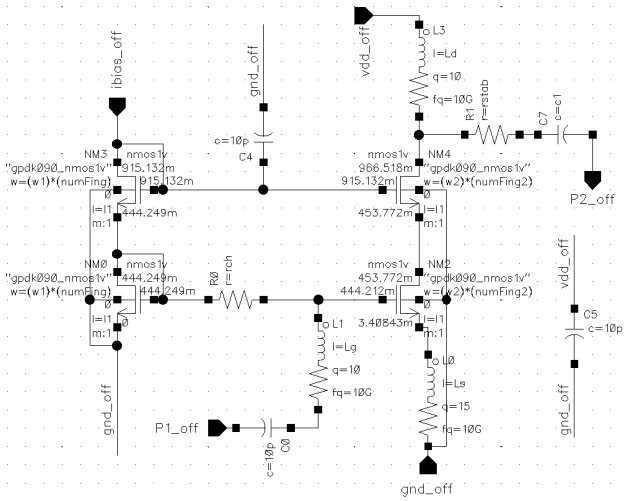


Figure 3: Intermediate LNA after following recipe but before adding the ASITIC inductors.

An additional note, the Q for the drain inductor was intentionally chosen low due to the bandwidth constraints on S_{22}. In previous iterations, it was found to be difficult to get S_{22} to stay under -10 dB over the entire bandwidth, even with a very good output match.

After matching the output, the stability was checked and it was found that K dipped below 1 at low frequencies. The recipe mentions a stability resistor in [2] and so some information on how to incorporate one was found at [5]. Adding this resistor allowed K to rise above 1 at the cost of G_{max}. If more time were available for exploration, a better method to achieve stability without a stability resistor would be investigated. The circuit at this stage of the design is shown in Fig. 3.

The final task was to replace the analogLib "indq" components with ASITIC inductors. Doing so brings the design to its final topology that is shown in Fig. 7. These inductors were designed to match the ideal inductors used up to this point. However, at this point in the design, if jiggling parameters and adding optimized ASITIC inductors did not meet specifications, the design was restarted with different geometries and other design choices. There was also a cycle of iteration that involved designing ASITIC inductors, simulating the LNA, jiggling available parameters such as reference current, geometries and C_1, then redesigning the ASITIC inductors. The process is summarized in Fig. 4 and is where most of the design time was spent. The ASITIC sweeps used to craft the inductors are provided at this link: ASITIC Sweep Results. The procedure for constructing the Cadence PI model was followed from [7]. Approximately 32 ASITIC models were created and used over all iterations.

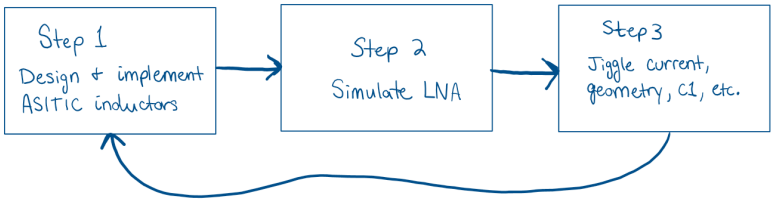


Figure 4: Final cycle of LNA design. Recommended to have a good base design before getting locked into this loop.

Step 3 in Fig. 4, was where the trade offs involved with the LNA were most notable. However, decisions with regards to trade offs in this design stage are detailed in Section 5.

3 Schematics - Component Values

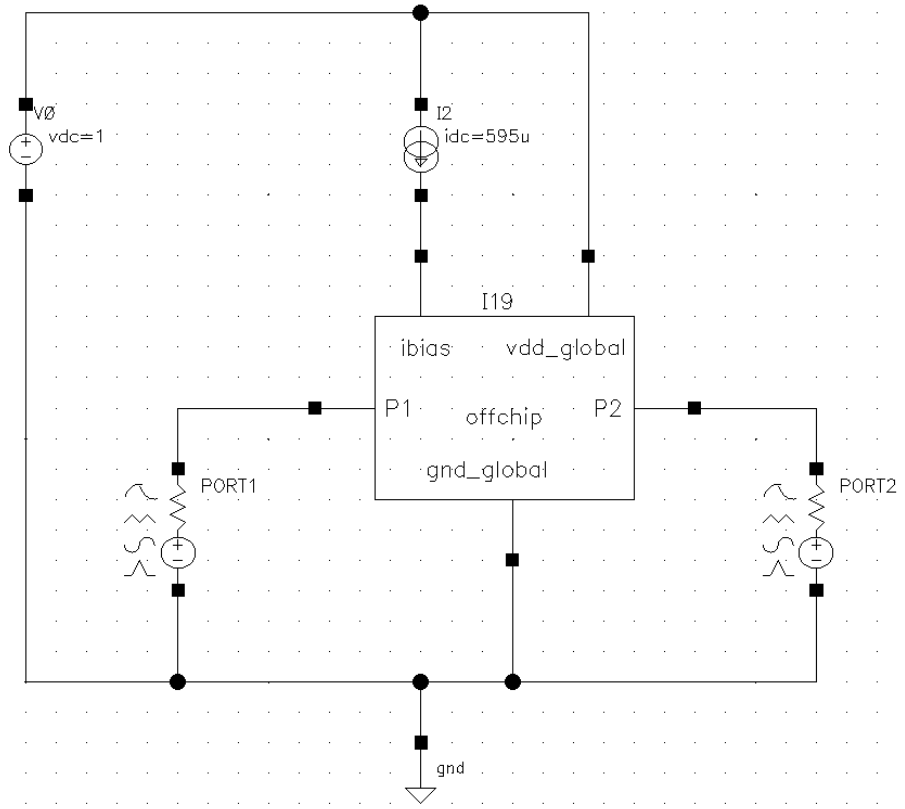


Figure 5: Test bench level of hierarchy with component values. Includes ideal voltage and current supply along with the input and output ports. This circuit contains global ground. The symbol "offchip" is shown in Fig. 6.

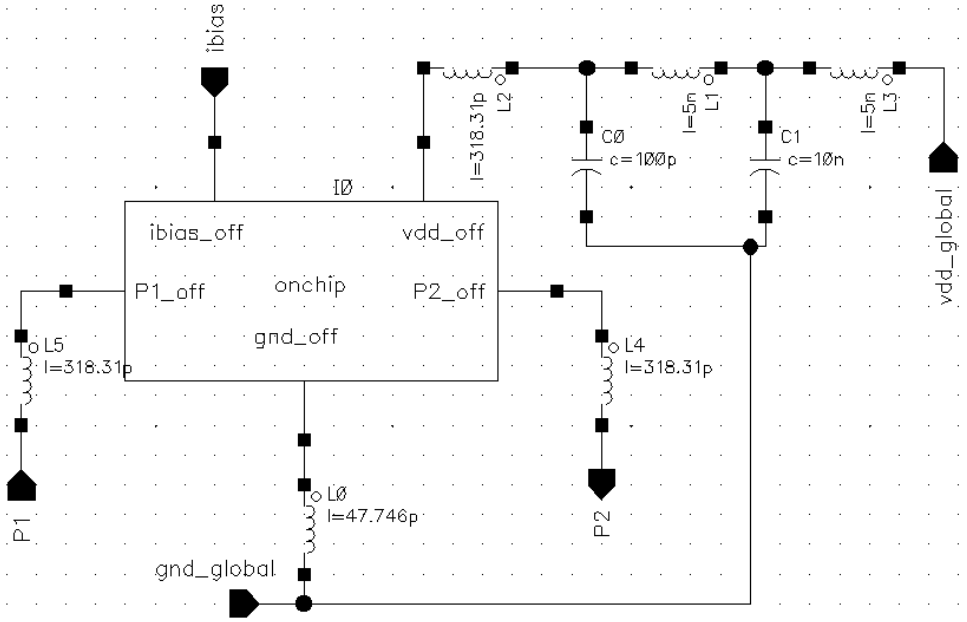


Figure 6: Offchip hierarchy with component values. Shows the parasitics that exist between the chip and supply, ground, and ports. The "onchip" is shown in Fig. 7.

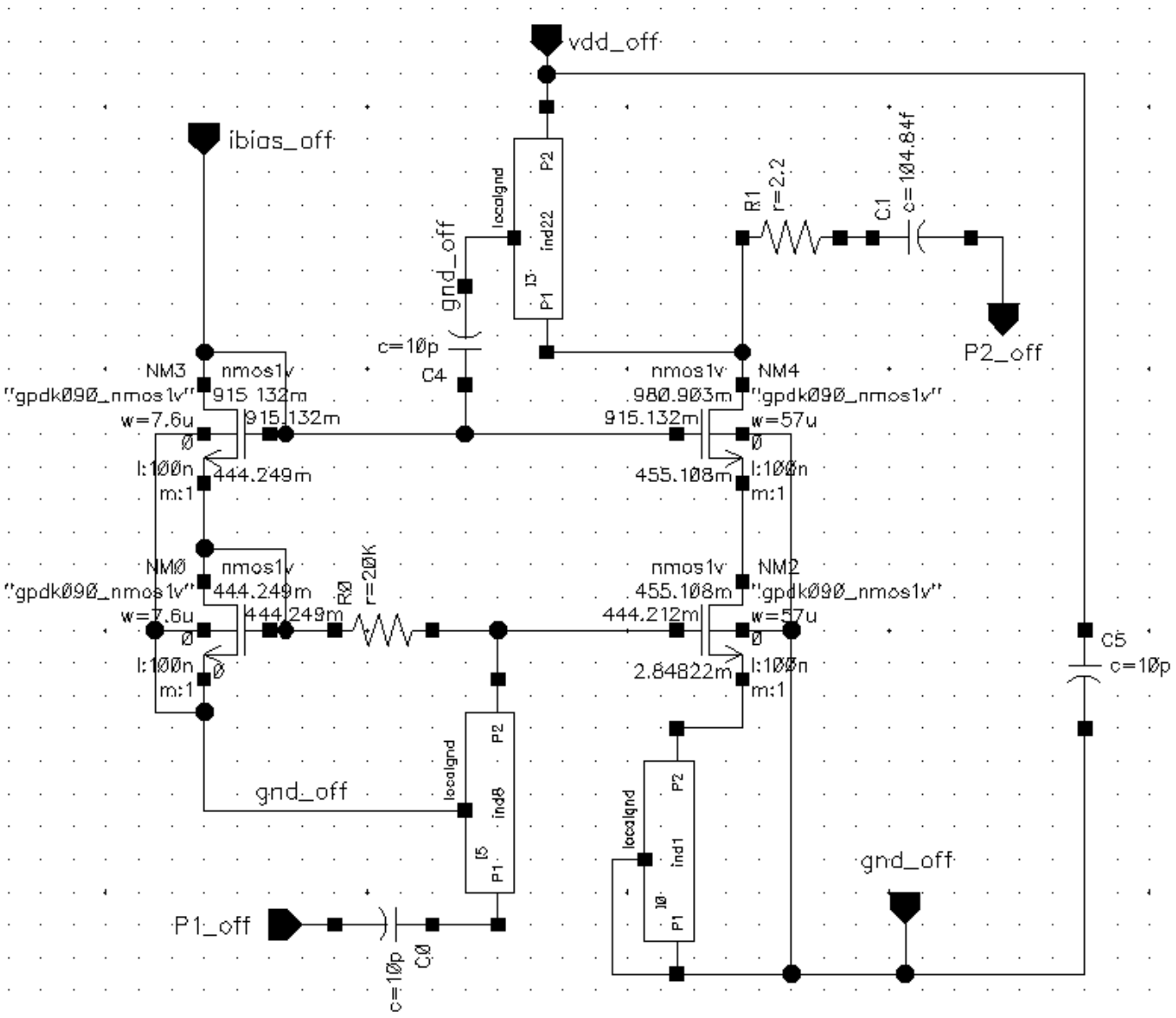


Figure 7: The "onchip" hierarchy with component values. This level uses a local V_{dd} and ground that is connected to chip parastics. ASITIC inductors ind1, ind8, and ind22 are shown in Fig. 8, 9, and 10 respectively.

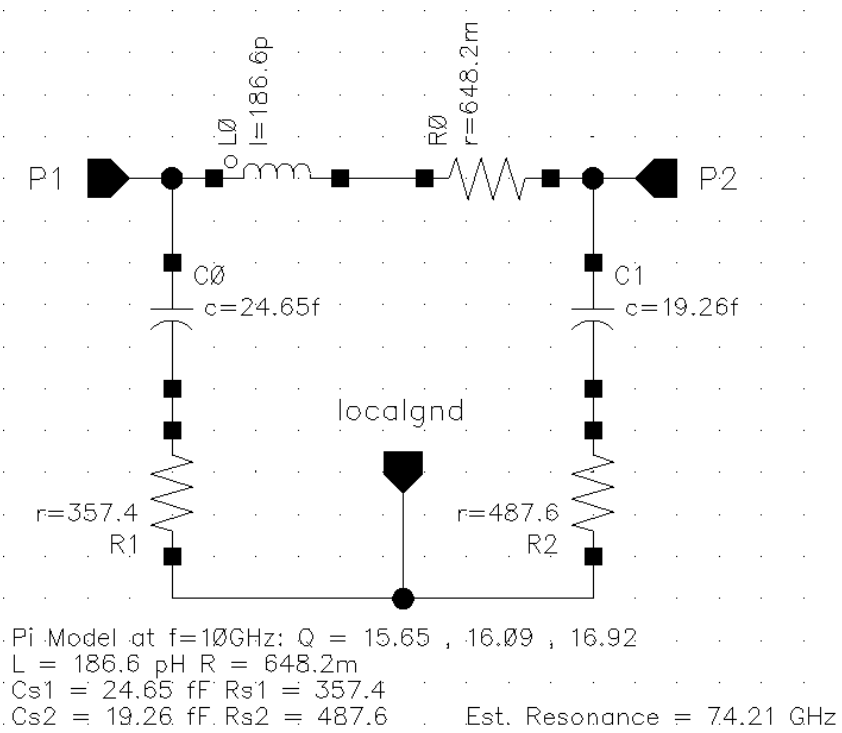


Figure 8: Source inductor PI model with component values. The parameters are shown in the figure.

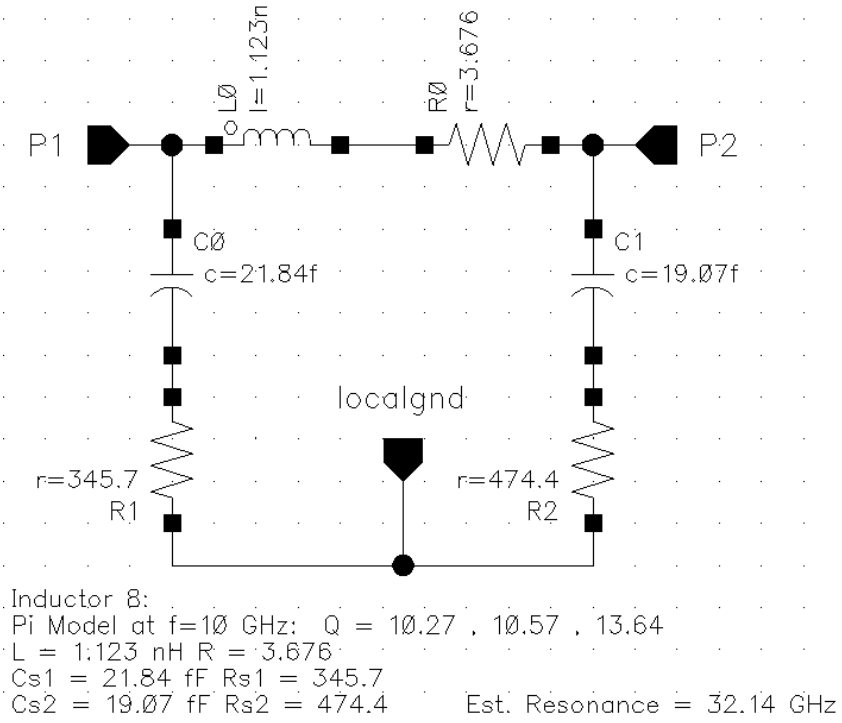


Figure 9: Gate inductor PI model with component values. The parameters are shown in the figure.

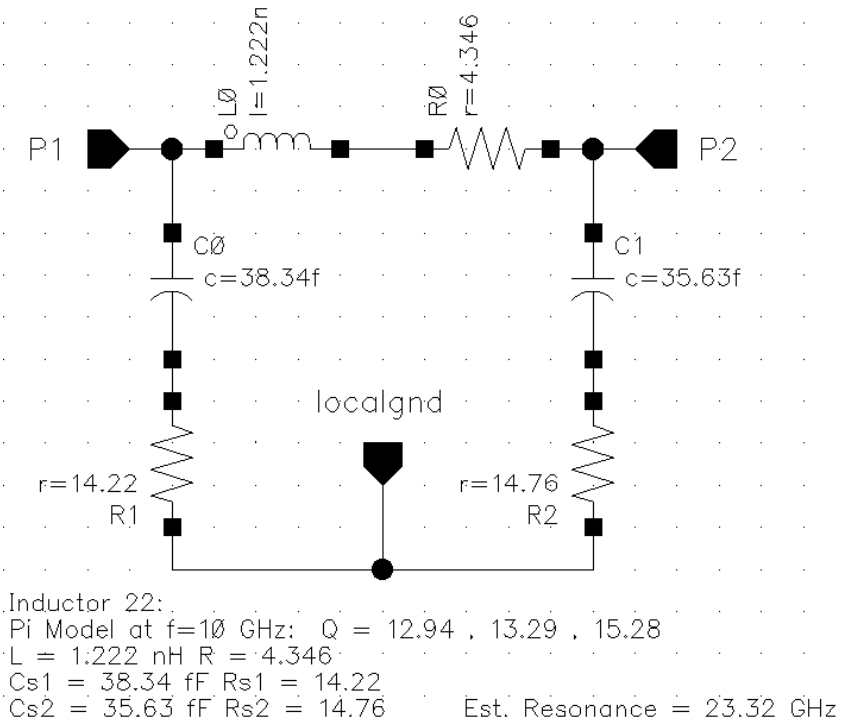


Figure 10: Drain inductor PI model with component values. The parameters are shown in the figure.

4 Simulation Plots

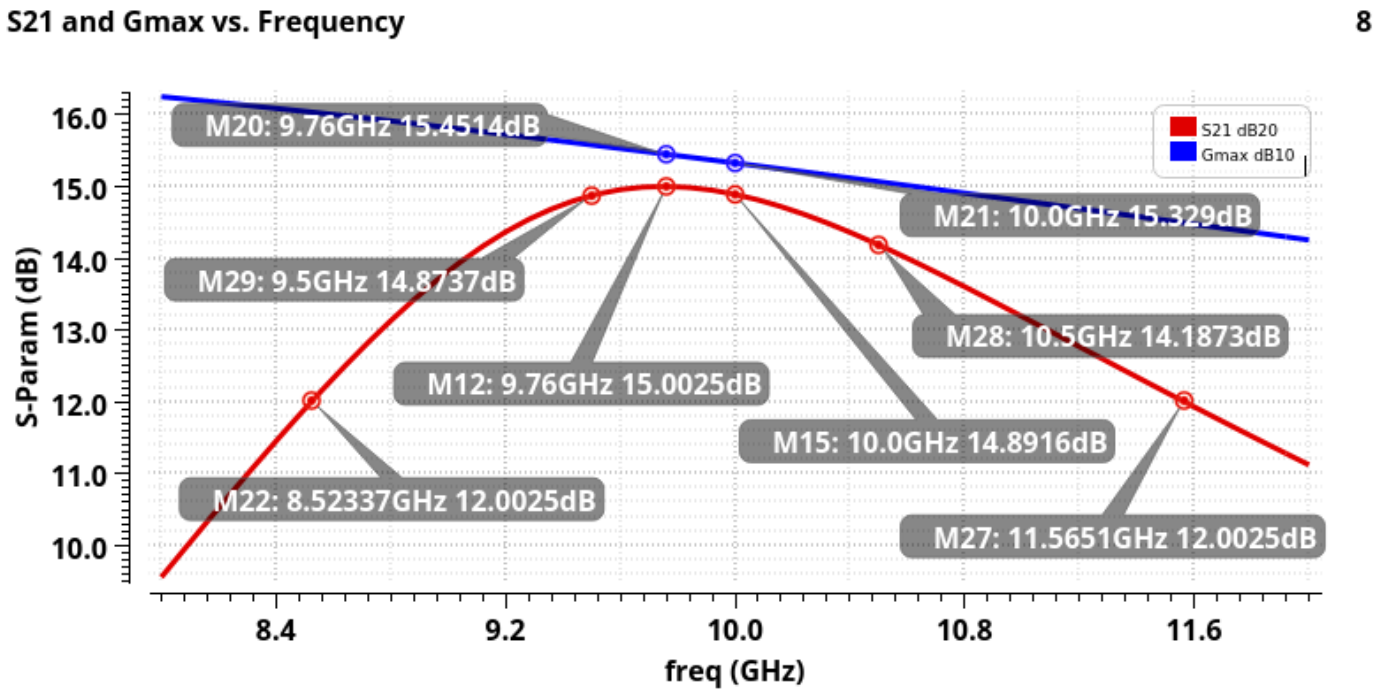


Figure 11: $|S_{21}|$ and G_{max} versus frequency. Both the 10% fractional bandwidth around f_c and the 3 dB bandwidth are marked on the plot. S_{21} peaks at 9.76 GHz. The gap between $|S_{21}|$ and G_{max} is due to input and output mismatch.

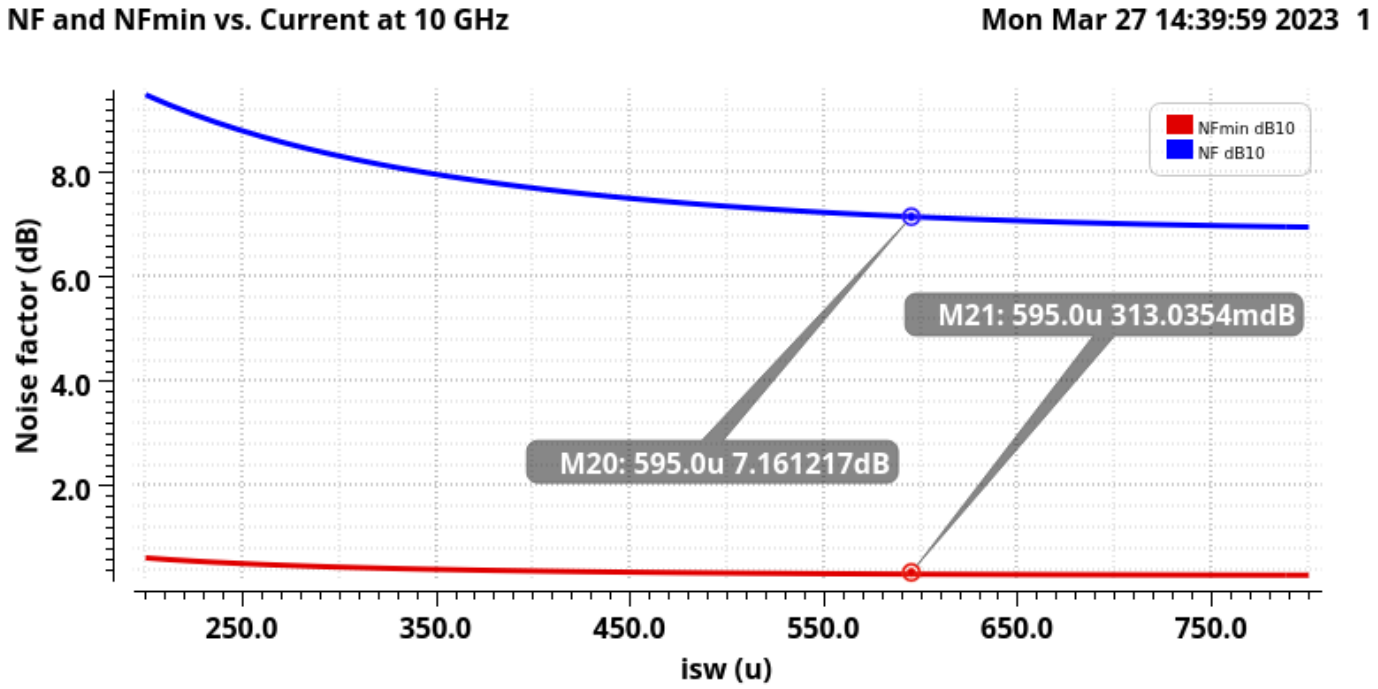


Figure 12: Noise figure and minimum noise figure versus current mirror reference current at 10 GHz. The noise figure is much higher due to Γ_{opt} not being matched yet. The NF_{min} at the chosen reference current of 595 uA is 313 mdB.

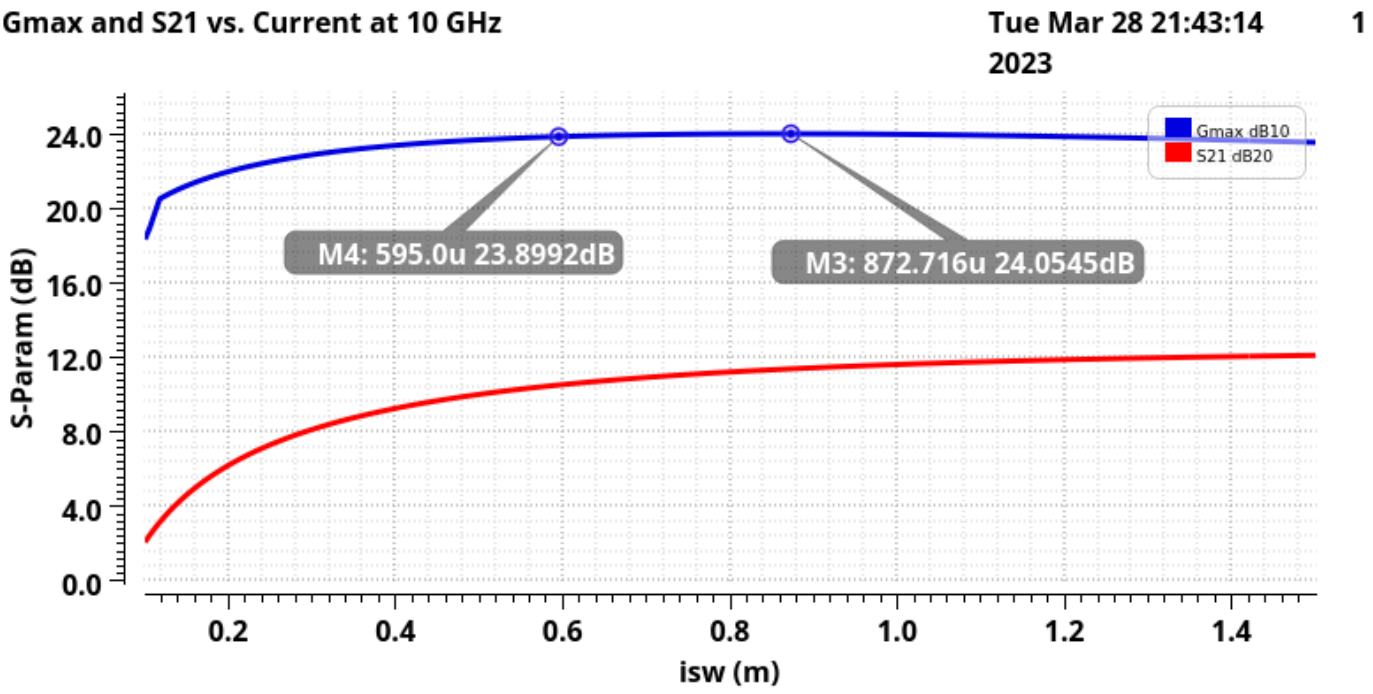


Figure 13: $|S_{21}|$ and G_{max} versus current mirror reference current at 10 GHz. G_{max} peaks at 873 uA, but 595 uA was chosen instead. G_{max} at 595 uA is 23.9 dB.

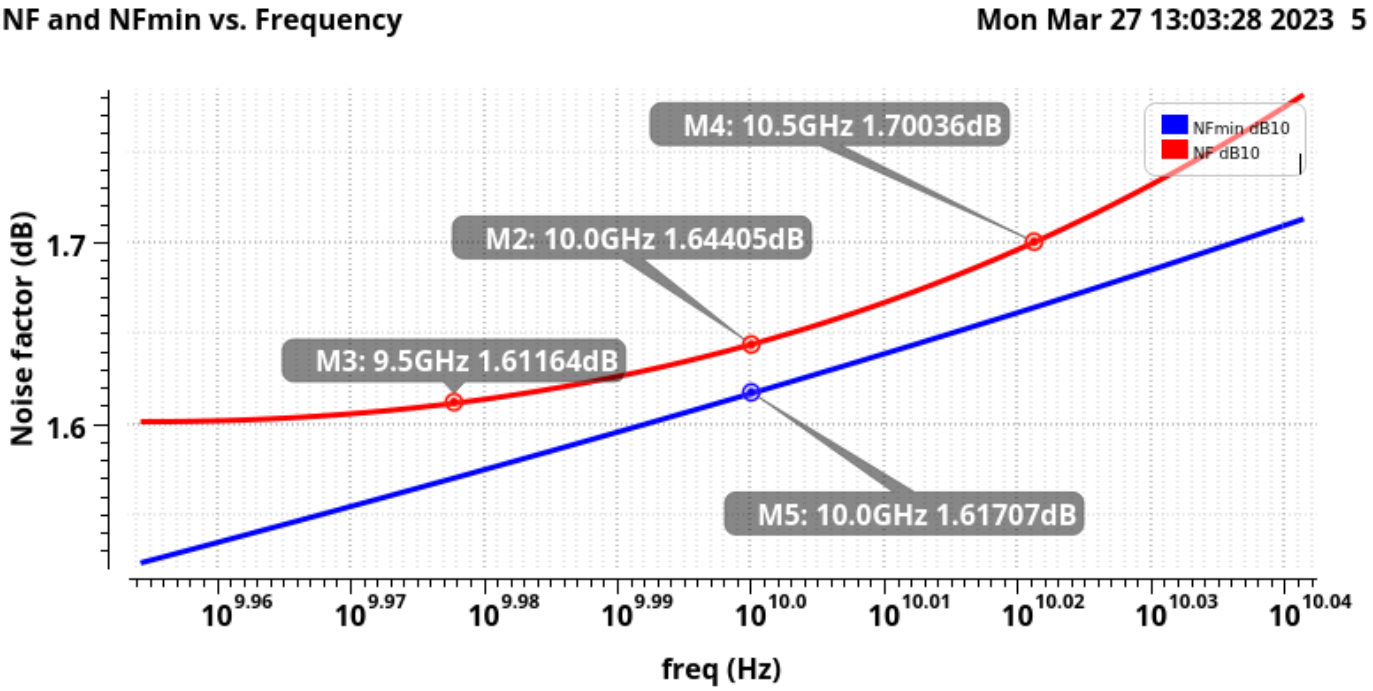


Figure 14: Noise figure and minimum noise figure versus frequency. Noise figure increases with frequency but never exceeds the 2.7 dB limit. The NF does not touch NF_{min} due to Γ_{opt} mismatch. The 10% fractional bandwidth is marked on the plot.

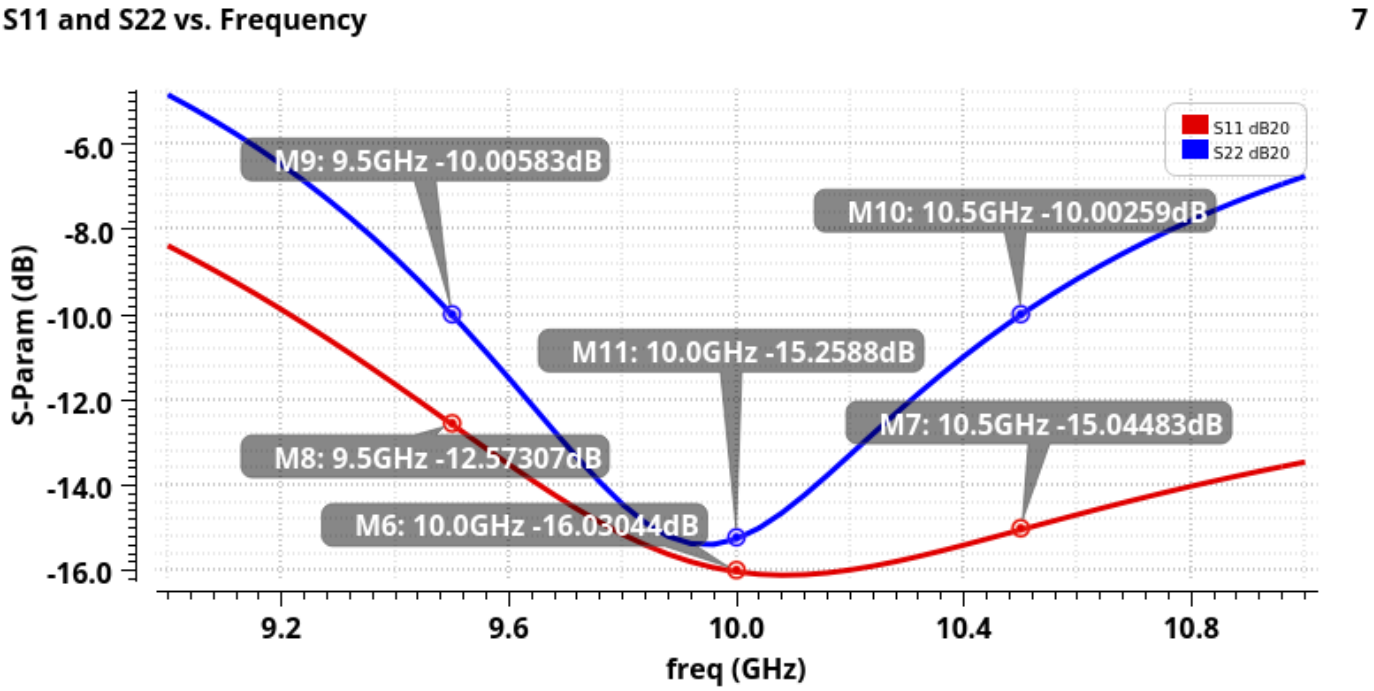


Figure 15: $|S_{11}|$ and $|S_{22}|$ versus frequency, barely staying under -10 dB. Both $|S_{11}|$ and $|S_{22}|$ are minimum close to f_c. The 10% fractional bandwidth is marked on the plot.

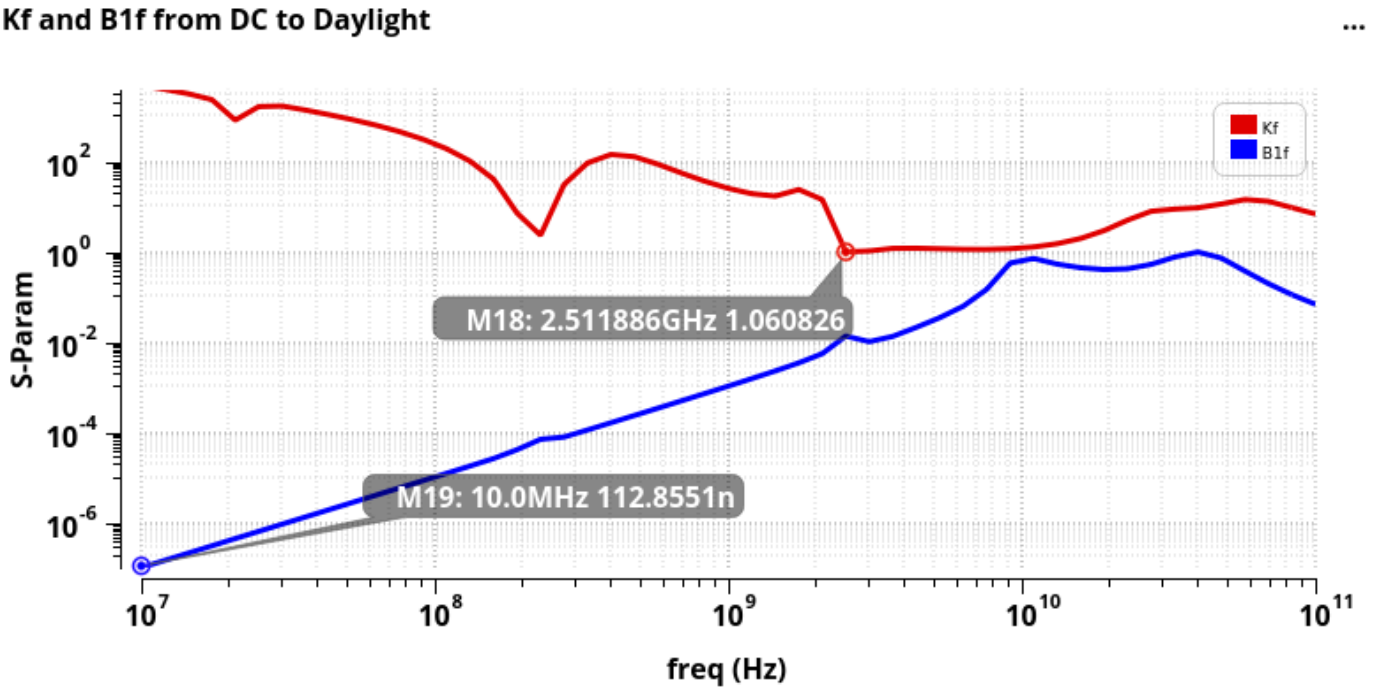


Figure 16: Stability factor K and B swept from 10 MHz to 100 GHz. K maintains above 1 and B maintains above 0 and thus resulting in unconditional stability.

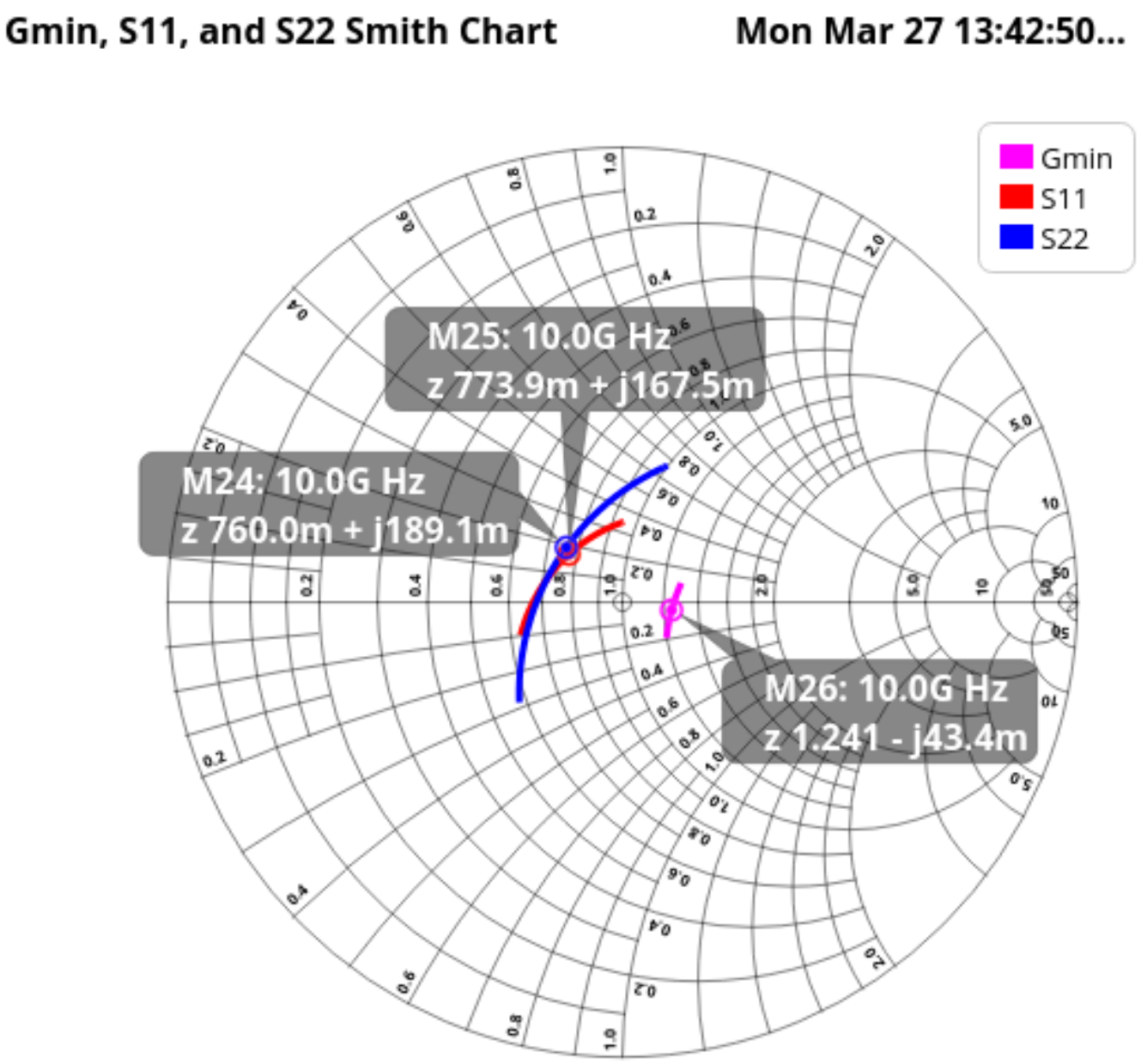


Figure 17: S_{11}, S_{22}, and G_{min} (equivalently Γ_{opt}) are swept from 9.5 GHz to 10.5 GHz, the 10% fractional bandwidth. The center frequency, f_c is marked on the Smith chart.

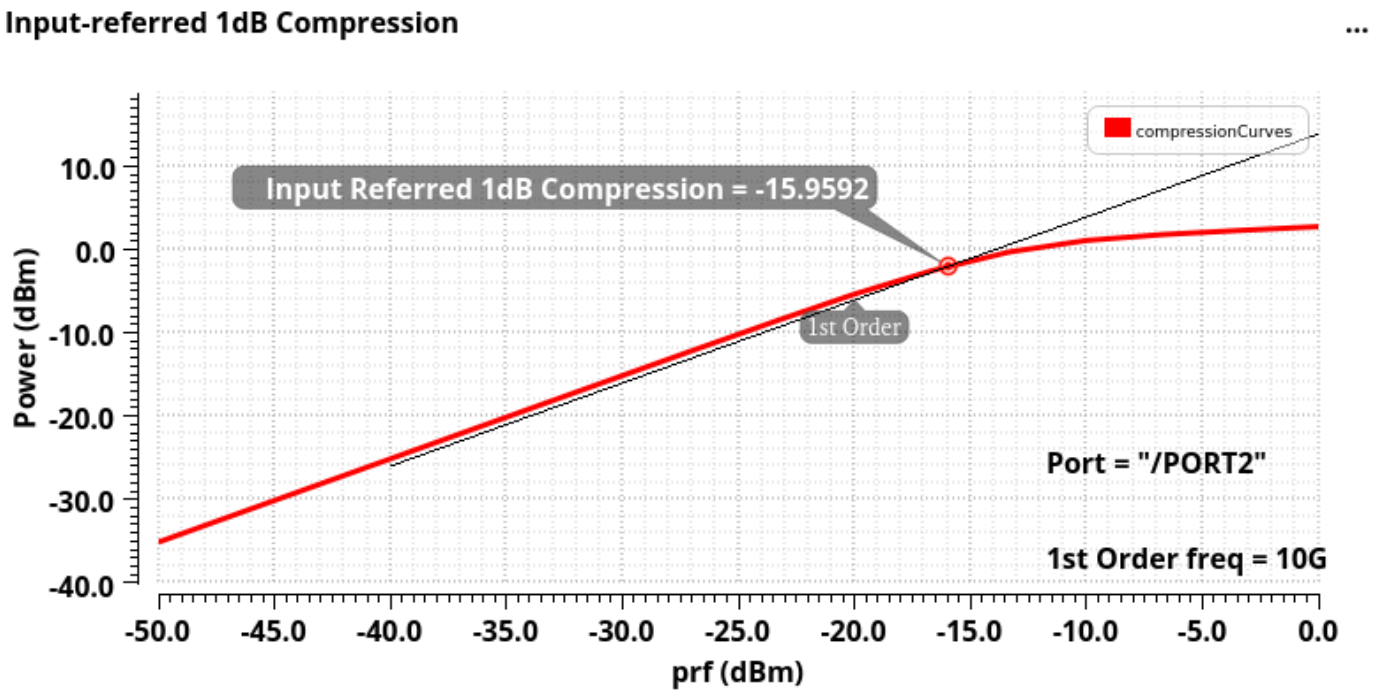


Figure 18: Output power versus input power. The 1st order line is 1 dB/dB and shifted down by 1 dB. When the 1st order line intersects the output power curve that is the point where the output power is 1 dB less than it would be if it were to keep at 1 dB/dB. This is the Input Referred 1 dB Compression.

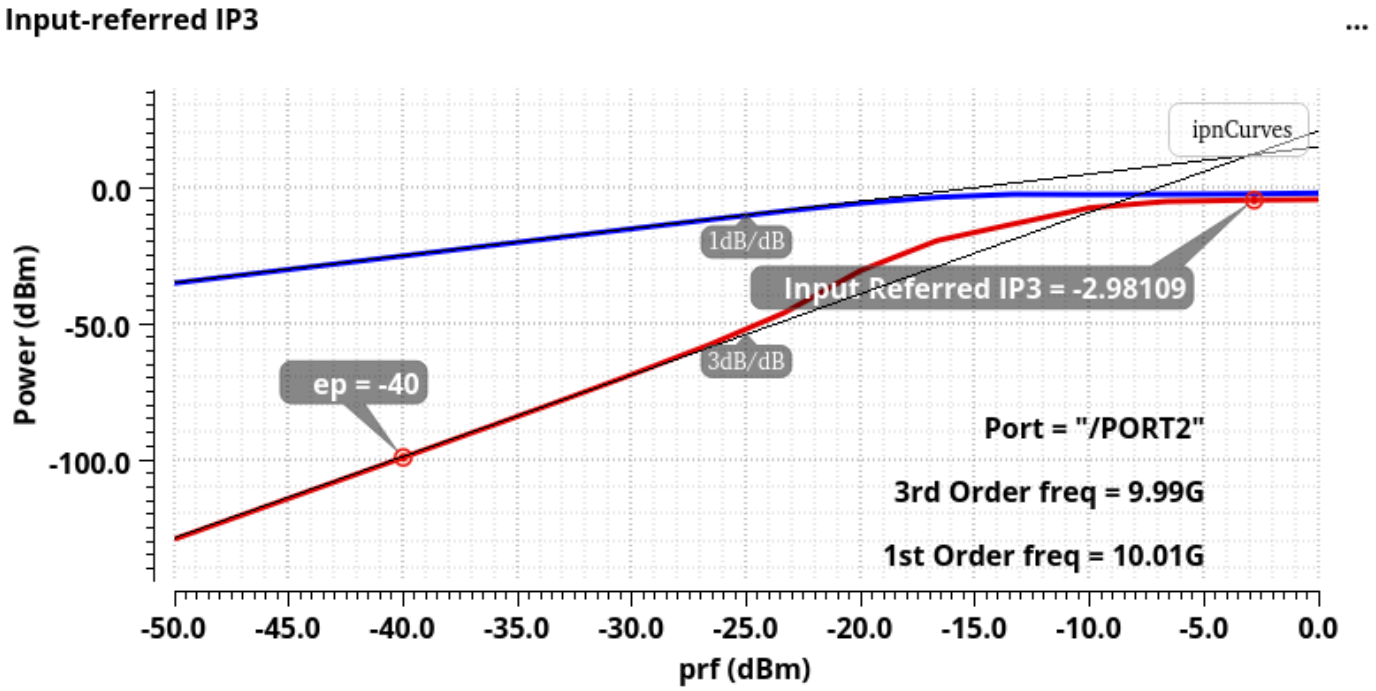


Figure 19: Output power versus input power. The 3 dB/dB line of the third harmonic and the 1 dB/dB line of the first harmonic are extrapolated to where they intersect. This is the Input Referred IP3.

5 Discussion

The LNA seemingly has an infinite number of trade-offs, but only a few are discussed here. The first important trade-off is the inductive degeneration's affect on gain and linearity. Having a larger L_S helps linearity but reduces gain. This effect can be minimized by having a high Q source inductor. This causes the inductor resistance to be lower, decreasing degeneration and improving gain. Lowering the parasitic resistance increases gain which allows L_S to increase to help linearity while lowering gain back to its starting point.

The next trade-off is from the inductance and Q value of the drain inductor. High inductance and Q at the drain is needed to help gain, but a high Q value causes the output bandwidth to decrease. The gain needs to be sufficiently high to account for a drop in gain due to a lower Q to support larger bandwidths. Due to gain being an issue in this design, a balance between meeting the gain and S_{22} was difficult to achieve.

The last trade-off discussed is between stability and gain. For this design, a stability resistor was introduced to raise K above 1. In doing so, gain was reduced. Without the stability resistor gain was much easier to achieve. Due to having a base design deficient in stability, the stability resistor was required and finding a balance between stability and gain was of concern in the final stages of the design process. In hindsight, further investigation into the cause of the instability would have been a better solution, that would have alleviated the pains of meeting the gain specification.

The only specification that was not met was the 1 dB compression point. At this time, the direct solution for having met this specification is not clear. It is known that care should have been taken to observe 1 dB compression over the entire design process. What is important for 1 dB compression is that the signal does not get clipped, has appropriate headroom, and that the DC operating point exist within a linear region.

The 1 dB compression was the last specification to be attempted. Due to the tiny wiggle room on the other specifications, the 1 dB compression was left as it is to maintain the other specifications. A wide-swing cascode was attempted and helped with IP3 and 1 dB compression, but with the time constraint, correctly implementing the wide-swing cascode while keeping the other specifications met was not achieved.

A few observations were made with regard to how to tackle the 1 dB compression point from the starting point of the submitted design. First, dropping the reference current to 300 uA brings the 1 dB compression to greater than -13 dB. However, this drops the gain below 15 dB, lowers IP3 below -3 dB, increases NF near the limit of 2.7 dB, and increases stability to the point that the stability resistor is no longer needed. This also drops power consumption far below 5 mW. This is expected as the operating point moves leftwards out of the non-linear region into a more linear region.

What this indicates, is that a lower current may have been a better choice, with power consumption dictated by choice of device sizing. The geometry would need to be altered to ensure the optimum current density exist at lower reference currents to help with noise figure.

The lowered IP3 could be combated using the source inductor. However, increasing source inductance would further decrease gain. Removing the stability resistor would help gain but is not enough to keep it above 15 dB. A re-look at the drain inductor would be required. The base design would need to be planned around a larger drain inductance, but with the trade-off in mind that a high Q may prevent meeting the S_{22} bandwidth requirement, so the impact of the previous changes on bandwidth would need to be observed to indicate how to handle L_D properly.

6 Conclusion

The LNA described in this document met all but one specification. The recipe in [2] was useful to get on the right track and to get a working cascoded common source LNA with inductive degeneration. However, there were non-ideal characteristics that the recipe did not account for, especially with regard to trade-offs such as gain and S_{22} bandwidth.

Admittedly, the most time was spent on tweaking parameters to meet the specifications. Although the underlying concepts were understood, not enough emphasis was placed on understanding how to leverage the theory to gauge trade-offs. One lesson learned is that considerable time shouldn't be dedicated to tweaking, but that the base design should be well designed first, and if tweaking does not work in short time, then re-evaluate the base design. Ultimately, try to get very close to each specification and to overshoot the specifications that can be leveraged in trade-offs later on.

A solid understanding of the ASITIC inductor impact was gained later in the design process. A recommendation for future designers is to play with the ASITIC software early on to get a feel for what is possible, and to let this influence how L_S, L_G, and L_D are chosen. Place ASITIC PI models in the circuit as the design progresses and tweak the parameters to understand their impact. In the end, very well optimized ASITIC inductors were required to meet the last few specifications. In hindsight, the design process would have been much quicker if effort had been put into optimizing the ASITIC inductors earlier.

The linearity checks were put off until the end. There was not much difficulty in achieving IP3, however the 1 dB compression specification was not met. It was not until later that it was discovered that headroom and the DC operating point characteristics played such an important role. The power consumption was at its limit and at the end of the design, once the other specifications were accounted for, it seemed impossible to achieve the 1 dB compression. In hindsight this specification should be checked somewhat often. There was mention of creating a separate test bench for output current versus input voltage, however time ran short. This is something that would be pursued if repeating the design.

Ultimately, the most important lesson learned was to not get distracted with tweaking values, but in stepping back and trying to understand what trade-offs exists and which ones are applicable in that moment and to use this knowledge to first achieve a solid base design that doesn't require hours of tweaking to get within specifications.

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[2] B. Floyd. (2023). Lecture 13: Low-Noise Amplifiers II [PowerPoint Slides]

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[7] B. Floyd. (2023). ECE 712 Spiral Inductor Analysis/Modeling with ASITIC [PDF Document]

A Schematics - DC Operating Point

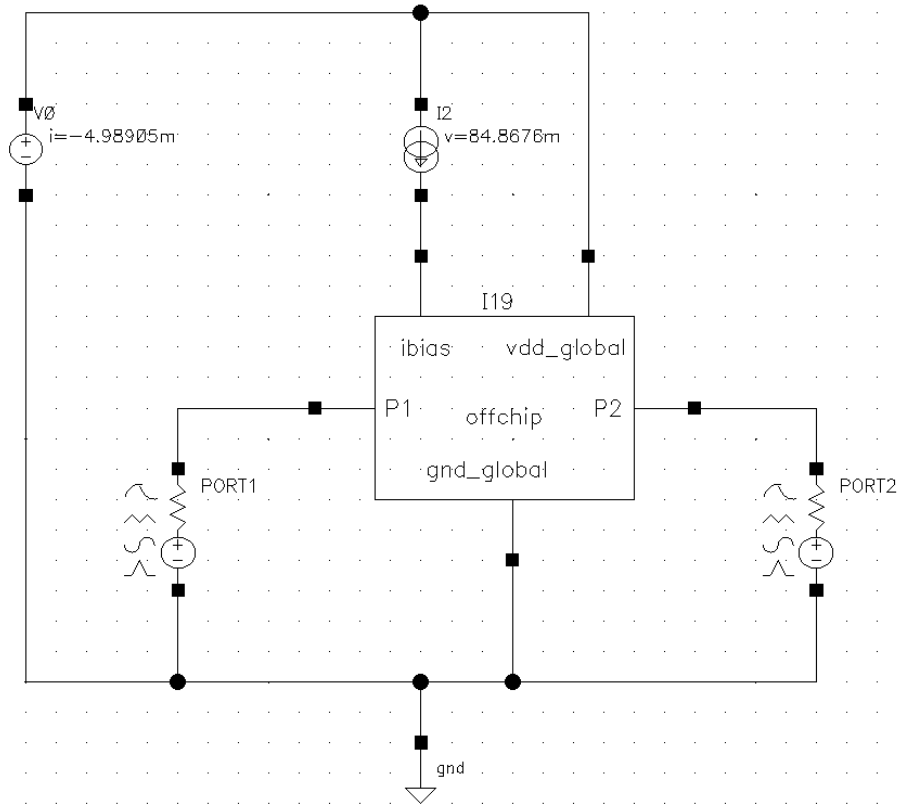

Figure 20: Test bench level of hierarchy with DC operating point values. Includes ideal voltage and current supply along with the input and output ports. This circuit contains global ground. The symbol "offchip" is shown in Fig. 21.

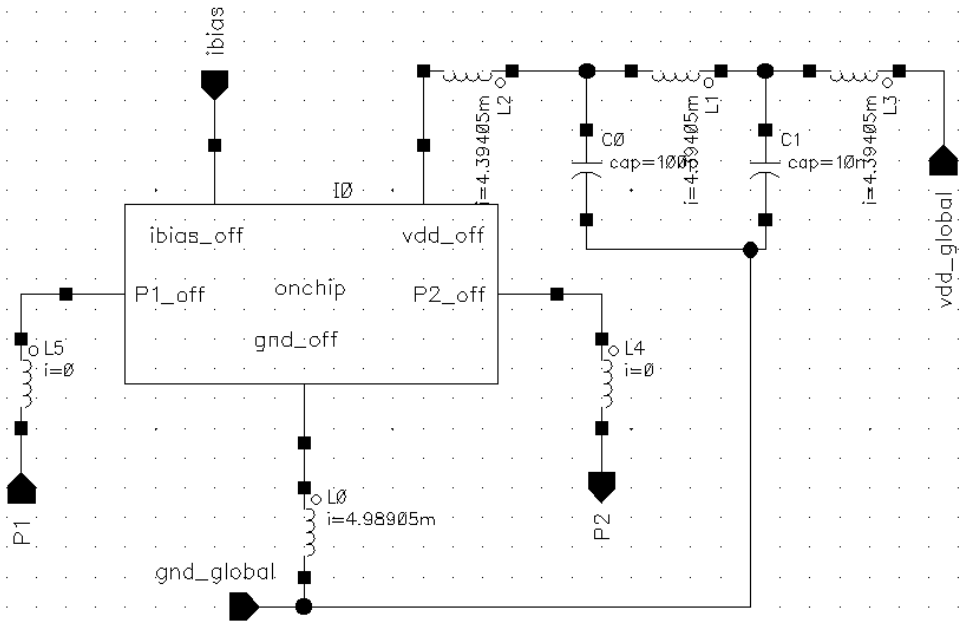

Figure 21: Offchip hierarchy with DC operating point values. Shows the parasitics that exist between the chip and supply, ground, and ports. The "onchip" is shown in Fig. 22.

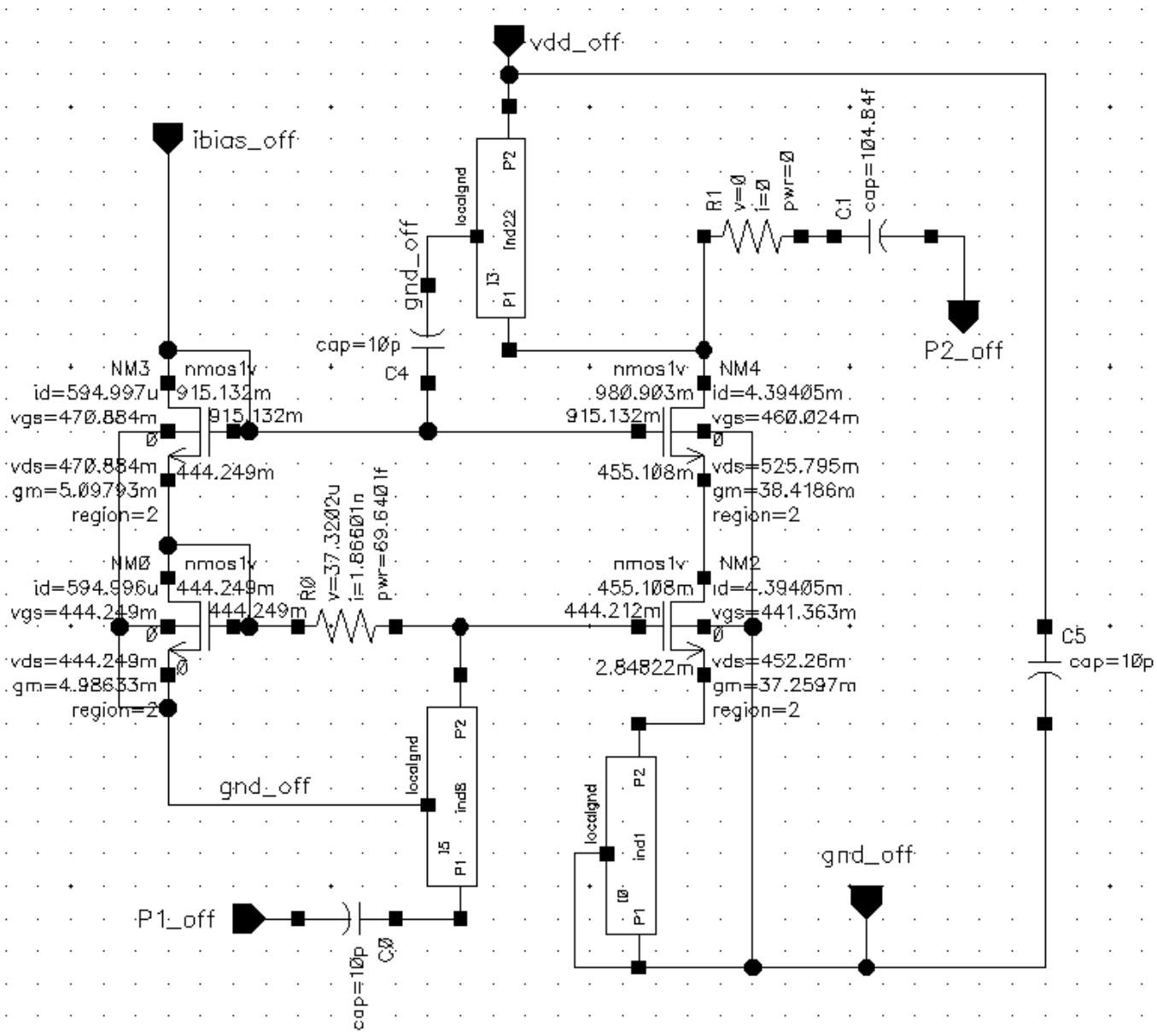

Figure 22: The "onchip" hierarchy with DC operating point values. This level uses a local V_{dd} and ground that is connected to chip parastics. ASITIC inductors ind1, ind8, and ind22 are shown in Fig. 23, 24, and 25 respectively.

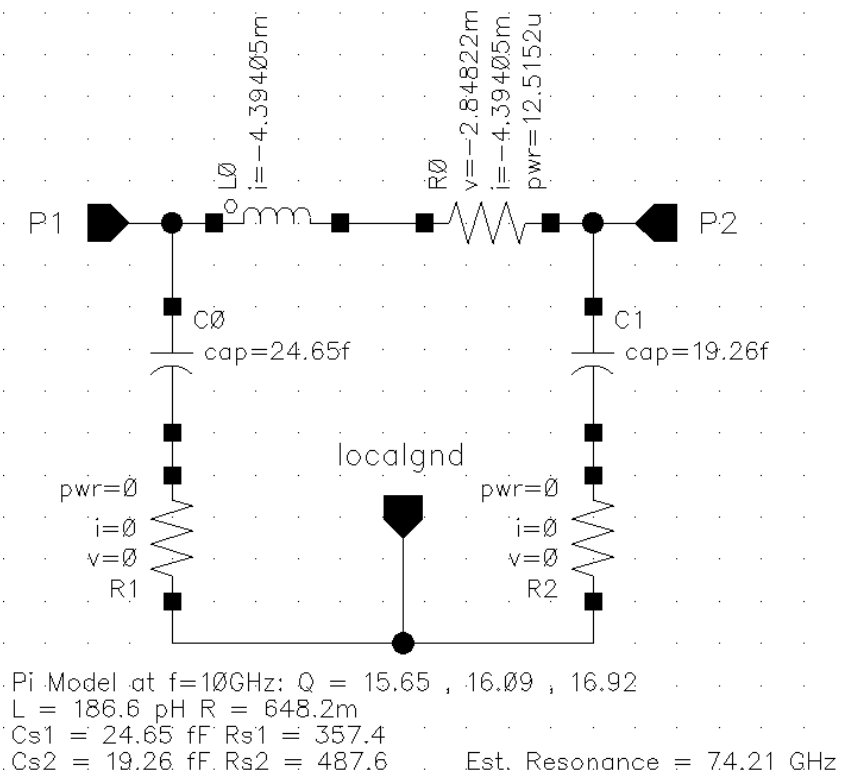

Figure 23: Source inductor PI model with DC operating point values. The parameters are shown in the figure.

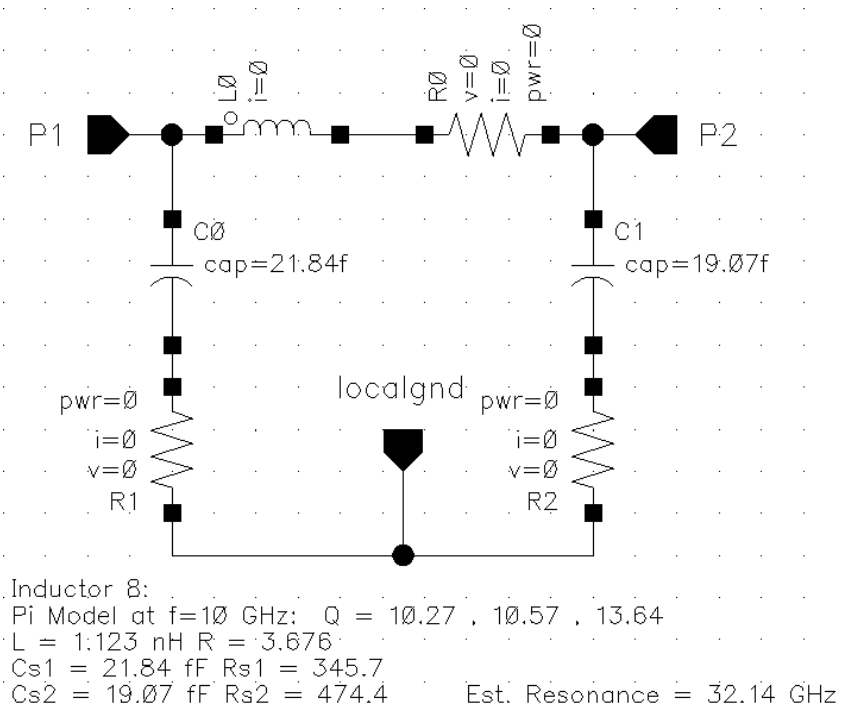

Figure 24: Gate inductor PI model with DC operating point values. The parameters are shown in the figure.

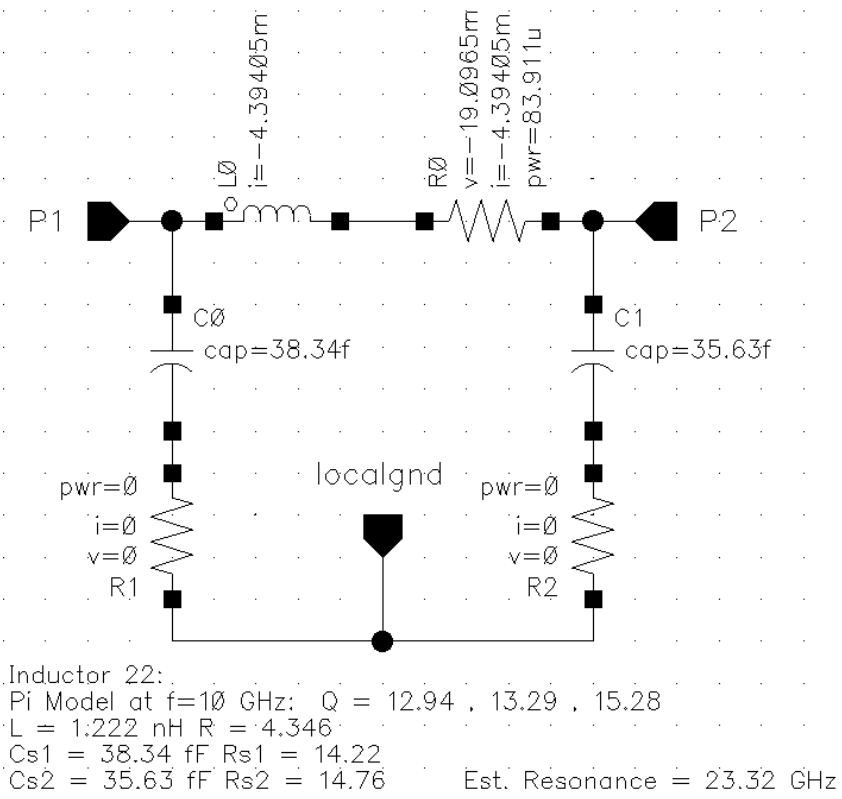

Figure 25: Drain inductor PI model with DC operating point values. The parameters are shown in the figure.