ECE 511 Design Project: Fully-differential OTA

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William T. Jarratt and Pryor A. Gibson pledge that all work contained within represents their team's own work and the work of nobody else.

1. Executive Summary

This document outlines the specifications of an Operational Transconductance Amplifier (OTA) and the design choices and tradeoffs that went into achieving those specifications. The required specifications are outlined in section 2, along with the actual specifications of the OTA.

This OTA is fully differentiable and able to achieve a minimum gain of 86 dB over an input common mode voltage of 0 V to 1.8 V and with a differential output swing of -0.8 V to 0.9 V at a nominal supply voltage of 2 V. The 3 dB bandwidth is 11.5 KHz, with a gain bandwidth product over 350 MHz. The OTA achieves a Common Mode Rejection Ratio (CMRR) of 125 dB at low frequencies, along with a Positive Power Supply Rejection Ratio ($PSRR^+$) of 270 dB. The OTA is internally compensated, providing a 80 degree phase margin of the overall OTA. Each internal feedback loop has a phase margin greater than 45 degrees. The OTA has a quick settling rate, at less than 5 nsec with very little ringing and a slew rate over 100 V/μsec. Unfortunately, this OTA does not have input-referred noise voltage floor less than 11 nV/$\sqrt{Hz}$ and is not recommended for low noise applications. The OTA draws less than 1mW of power.

Section 3 provides an in depth technical discussion of OTA high level design and architecture, along with the subcomponents. The topology of the supply-independent bias current generation, the gain-boosting stages and their device sizing and performance is analyzed. Additionally, the methods used to compensate and achieve stability for the main OTA, Common Mode Feedback (CMFB), and other internal loops are discussed. Lastly, the technical discussion provides a look into the tradeoffs encountered during simulation and design, and reasoning for the choices made.

Sections 4 and 5 provide the hierarchical schematics of the OTA, beginning with the level of hierarchy starting at the test bench, moving down into the OTA that contains the CMFB, PMOS active cascode, NMOS active cascode, and supply independent levels. Section 4 references the schematics, showing the device and element sizes. Appendix A includes the same schematics, but with the DC operating conditions instead of the sizes. The DC operating conditions include the operating region, g_m, Vds, Vgs, and Id.

The document ends with a conclusion that details what could have been done to further improve performance of the OTA, highlighting results that indicate what next steps or tests would be required.

2. Compliance Table

Parameter	**Required Specification**	**Characterization**
Low frequency gain	92 dB (39800 V/V)	92.86 dB
Gain-Bandwidth Product	>350MHz	366.99 MHz
Phase margin	80 for OTA, internal feedback and CMFB <PM>(<Phase>)	Overall: 81.557 (-98.443) CMFB: 51.792 (51.792) PMOS: 89.505 (+90.495) NMOS: 90.525 (-270.525)
Settling time (1% of final value)	<100 nsec driving the compensation cap	4.85 nsec
Output Swing	2.4 volts p2p differential	1.807 V
Input common-mode range	At least 0.8-V overlap with output signals	0.0 to 1.84 V full range 0.0 to 907.284 mV overlap
CMRR	>100 dB	126.37 dB
$PSRR^+$	>90dB	271.86 dB
Nominal supply voltage	2V	2V
Power dissipation of OTA	P_{diss} < 1mW	0.996 mW
Slew Rate	>30 V/μsec	410.67 V/μsec
Input-Referred Noise Voltage Floor	<11 nV/$\sqrt{Hz}$	13.1948 nV/$\sqrt{Hz}$

3. Technical Discussion

3.1. High Level Design Choices

At the highest level, in Figure 4.1 and Figure A.1, a current mirror (CM) OTA topology was chosen. As laid out in lecture 18 [1], the CM OTA was conceptually simpler to get started with and working and at the outset had an extra degree of freedom in choosing K, the mirror ratio from the input leg to the output leg. The device has an excellent input CM range and benefits from a higher output swing. The CM OTA does suffer from lower gain, secondary poles and bandwidth. Trading off between gain, bandwidth, and the secondary pole, lead to difficulty with the overall phase margin. This ultimately diverted focus from the CMFB and output swing.

By the time focus was reapplied to the stability of the CMFB and output swing, there was a tradeoff decision made for overall OTA phase margin and power consumption. Immediate changes to the CMFB circuits would drop gain from 92.8 dB to below 92 dB. The device sizing at the output leg was locked in due to its influence on the bandwidth and overall OTA phase margin. The current could not be increased due to power consumption and could not be decreased due to the influence of PM10's and PM1's Gm on gain and bandwidth. Ultimately, time ran short, and the CMFB was not able to be improved. Next steps for CMFB are detailed in the conclusion. Additionally, the NMOS active cascodes had poor performance when stability was checked and this was another attack vector for OTA performance improvement.

3.2. Device Sizing and Biasing

Device biasing was based on providing the best input and output swing and to ensure the proper current biasing was provided. The voltage biasing was handled by the bias generator subcircuit and was based on sizing the width and length ratios of the two transistors to provide the correct gate voltage that would give the proper current. The PM2 gate voltage in the main OTA was chosen to be high to allow a higher input DC voltage and the saturation voltage of NM2 in the main OTA was chosen to be small to allow all the drain voltage of PM10 to be small. Additionally the saturation voltages of the output legs were chosen to be around or smaller than 200 mV. The thought process was that when CMFB was operating properly, the output swing for each leg would be limited from 0.4 V to 1.6 V, or a 1.2 Vp2p output swing which would correlate to a 2.4 Vp2p differential output swing.

Sizing and biasing of the wideswing cascodes was the most difficult part of initially getting the CM OTA operational at above 60 dB. Before the PMOS active cascodes were added, the gate to PM5 and PM3 in the main OTA were biased with an ideal voltage source. This bias voltage was required to be within a small window that was set by the difference between the saturation voltage of PM6/PM4 and the threshold voltage of PM5/PM3. The initial design called for a PM5/PM3 biasing voltage between 1.343 V and 1.41 V. This was the last step needed to reach saturation on all transistors and achieve high gain with the CM OTA. After the initial sizing, devices were sized when trying to alter output capacitance and resistance, device transconductance (g_m), and device currents.

3.3. Intermediate Deadline Results

Intermediate deadline 1 was a simple common source amplifier and a parameter extraction. The purpose of this deadline was to get familiar with cadence and to gain a deeper understanding of device parameters and the relation between back of the envelope calculations and simulations. The conclusion is that back of the envelope equations are a good way to understand how things change and by what order, but are not going to achieve the final goal. Since the extraction was carried out for a specific geometry and DC operating condition, the extracted parameters were not accurate, but did give an order of magnitude approximation. It was more effective to use the DC operating condition annotation in Cadence.

Intermediate deadline 2 provided the basis for the test bench and the understanding of how to test single ended amplifiers. This amplifier was an NMOS input with a gain of over 28 dB and a 3 dB bandwidth above 300 MHz. This differential amplifier also provided a way to understand the relation between the bandwidth, input range, and gain trade off. Ultimately this design was not implemented in the final design. The simple current mirror active load amplifier was replaced by a current mirror OTA. Though the ideas dealing with the trade offs similarly applied.

Intermediate deadline 3 provided the most utility for the final design. The deadline 3 constant gm bias generator consumed 150 uA and only provided bias voltages for a regular cascoded NMOS and simple PMOS current mirror. The design was incorporated directly into the design and built upon. The original design generated a reference current of 50 μA, but was not needed and so was dropped to lower power consumption. This is detailed more in a later section. A chain of NMOS and PMOS current mirrors were added at low currents to allow for generating optimum voltages in the OTA. The deadline could only have been more useful if it incorporated trying different methods for generating optimum voltages.

3.4. Constant g_m Supply Independent Bias Generation

The bias generator is shown in Figure 4.4 and Figure A.4. This is a constant g_m bias generator that has the bias resistor attached to the PMOS devices and is found in lecture 13 [2]. The PMOS device PM2 attached to this resistor R1 has its body tied to its source and not VDD. This was done to eliminate the body effect and reduce mismatch between PM1 and PM2. A cascoded NMOS pair was used instead of a feedback loop to improve efficiency because at that stage of development, a smaller op-amp was not available. Devices are sized to provide a reference current of 30 uA using a bias resistor of 8.55 KΩ. The bootstrapper uses an inverter where PM0 is sized much smaller than NM0 to allow the inverter to change states at a voltage well below the voltage of higher gate voltage of the NMOS cascode pair.

The design strategy for the setpoint and bias voltages was to first use an ideal voltage source that could be sweeped and tuned to improve the OTA performance. Using an ideal voltage source allowed for focus on the main OTA topology. Once the main design had been finished and the known DC operating point was known, the bias voltages were constructed using low current legs with specifically sized devices and resistors. The resistors allowed for a

degree of freedom with device sizing to achieve a specific voltage. This was to accommodate critical device sizes in the main OTA and subcircuits.

3.4. Active Cascode Gain Boosting

Active cascodes were chosen as the method to boost gain. The gain of the smaller op-amps is directly multiplied into the output resistance. The design began with separately building the NMOS and PMOS active cascode circuits. The design was based on the design presented in lecture 18 [1]. The NMOS and PMOS both were designed to operate at similar voltages that were currently present in the CM OTA before adding gain boosting. The NMOS and PMOS active cascodes had greater than 25 dB of gain prior to being inserted. The NMOS pair was added first, with negligible effect. This was due to the upper output resistance limiting the total output resistance. After adding the PMOS pair, the gain jumped to approximately 97 dB. It was also noted that the active cascodes allowed an extra degree of freedom in choosing voltages in between the cascode pairs in the output legs, as the set voltage for the PMOS active cascodes was not as restricted as the direct gate bias voltages.

At some point, while adjusting the main OTA topology to achieve another specification, the NMOS active cascode suffered performance loss and exhibited poor loop gain and weird phase fluctuations. It is believed that a focus on understanding the performance of the NMOS active cascode would be the right first step to further improving the OTA performance.

3.6. Compensation of the Main OTA and Feedback Loops

Compensation was needed to assist the phase margin from inverting before the OTA reaches a 0dB gain. The initial phase margin was -20 degrees. At first the tail current was at 50 uA and the initial course of action was to compensate for the output. However, this caused the bandwidth to fall below specification. What was required was a way to increase the input leg Gm without adding capacitance. This was achieved by increasing the tail current and the width to length ratio of the input transistors. Cutting power consumption in the biasing circuitry and allocating it to the tail allowed the GBW and gain to be increased enough to meet the specification with a lead compensation capacitor and resistor. The increased gain from increasing the input leg Gm also allowed decreasing of output leg geometry which also helped to decrease the output leg capacitance.

Additionally, it was found that the active cascodes were causing issues with the phase of the overall OTA and so compensating the active cascodes also helped a great amount with achieving an overall phase margin greater than 90 degrees.

3.7. Common Mode Feedback Loop Gain and Stability

For CMFB, topology 4 was chosen from lecture 22 [4]. This topology seemed to have a simple mechanism for improving operation and was easy to understand. The loop gain of the CMFB is 8900, which is very good, but only has a phase margin of about 53 degrees. The CMFB is stable. The phase margin is likely only that good due to compensation efforts of the main OTA phase margin.

Quite a bit of time was wasted chasing saturation voltages and bias voltage decisions trying to increase output swing. This was due to an insufficient understanding of the impact of CMFB on the output swing. This quest for lower saturation voltages caused the width to length ratios of NM3, NM4, NM5, and NM6 to be large, with small overdrive voltages. However, performance of the CMFB circuit relies on the overdrive voltages of those NMOS transistors to be large and the overdrive voltage of PM0 to be small. Once this mistake was rectified and the proper overdrive voltages were applied, the output swing increased from 1.2 V to 1.8 V. This was a major obstacle.

4. Schematic Set 1

4.1. Overall Schematic with Hierarchy

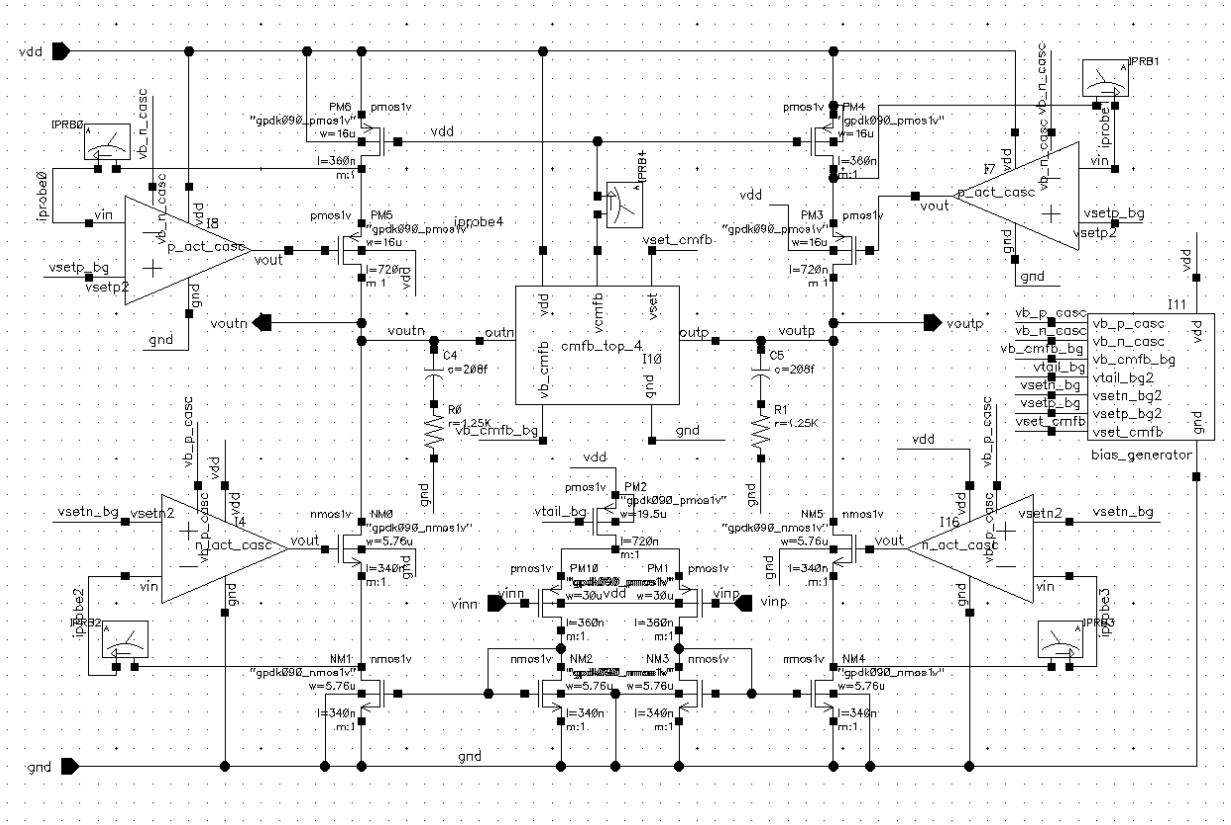

Figure 4.1: High Level Design of the OTA.

4.2. Active Cascodes

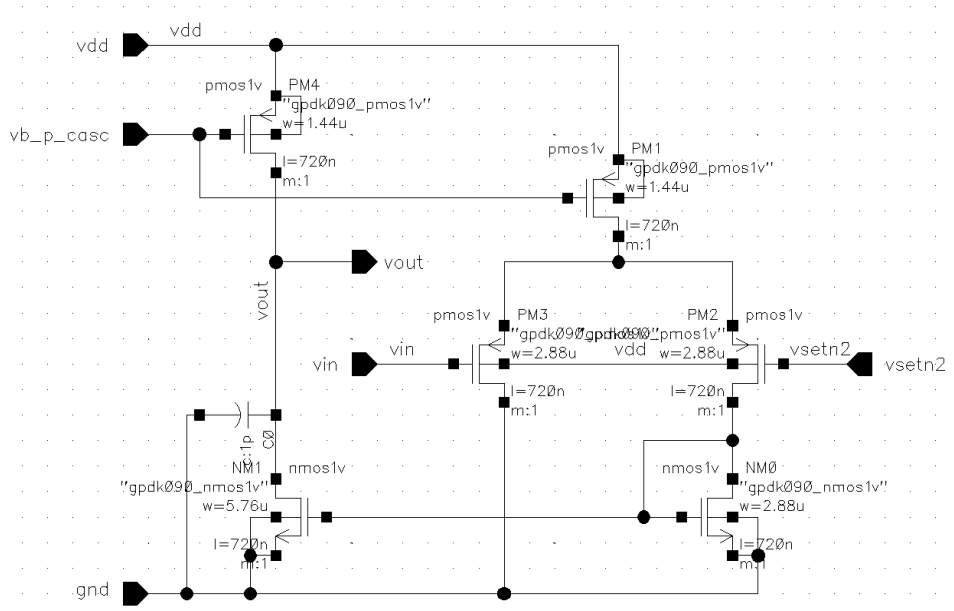

Figure 4.2: Schematic of the NMOS Active Cascode Circuit

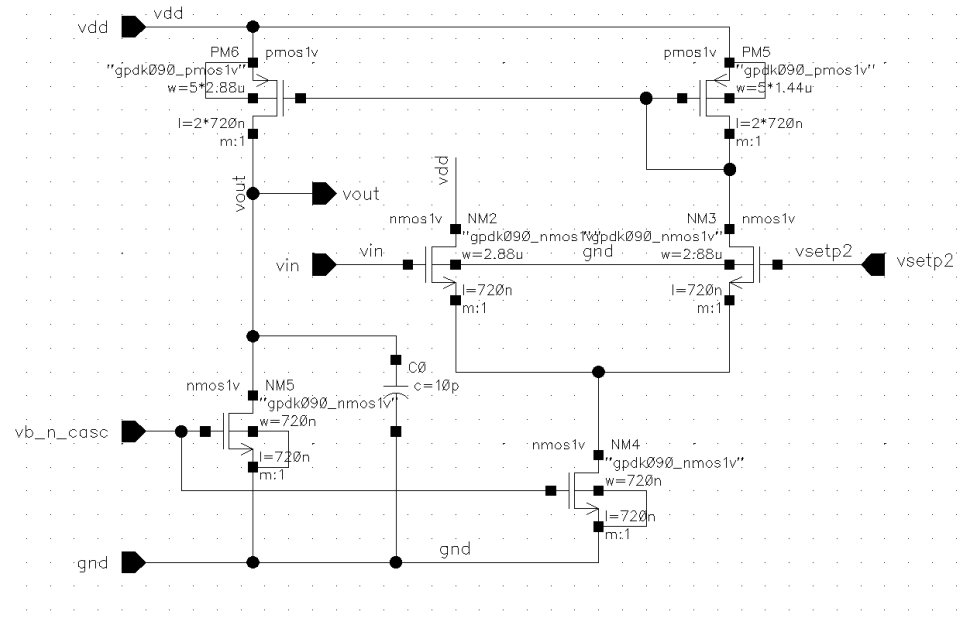

Figure 4.3: Schematic of the PMOS Active Cascode circuit.

4.3. Common Mode Feedback (CMFB)

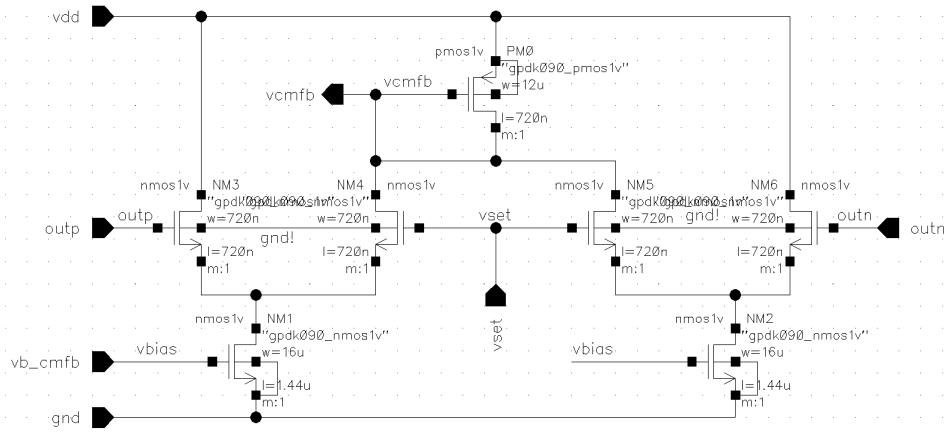

Figure 4.4: Schematic of the CMFB Circuit.

4.4. Constant gm Biasing Circuit

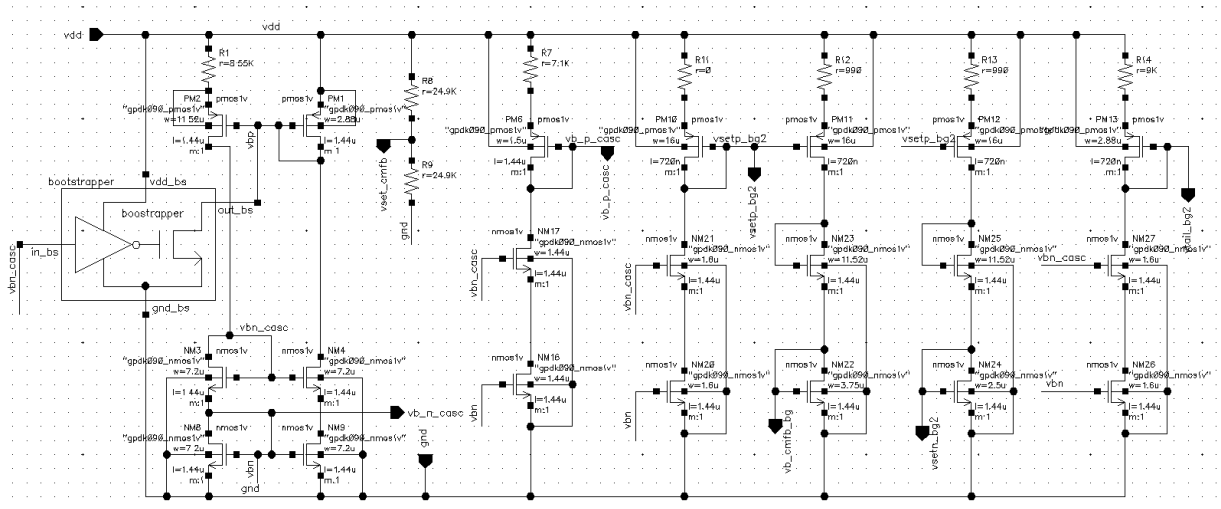

Figure 4.5: Schematic of the Current-Controlled Biasing Circuit.

4.5. Bootstrapping Circuit

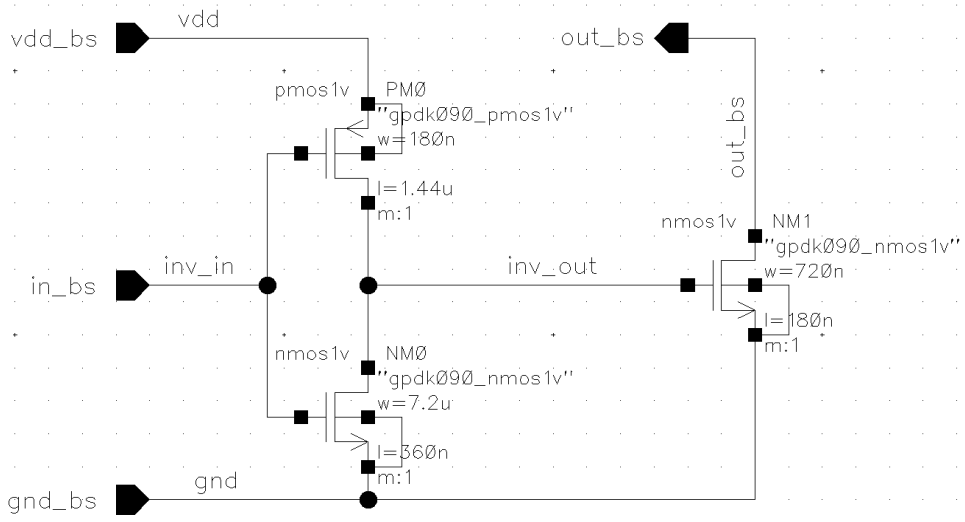

Figure 4.6: Schematic Bootstrapping Circuit.

4.6. Test Benches

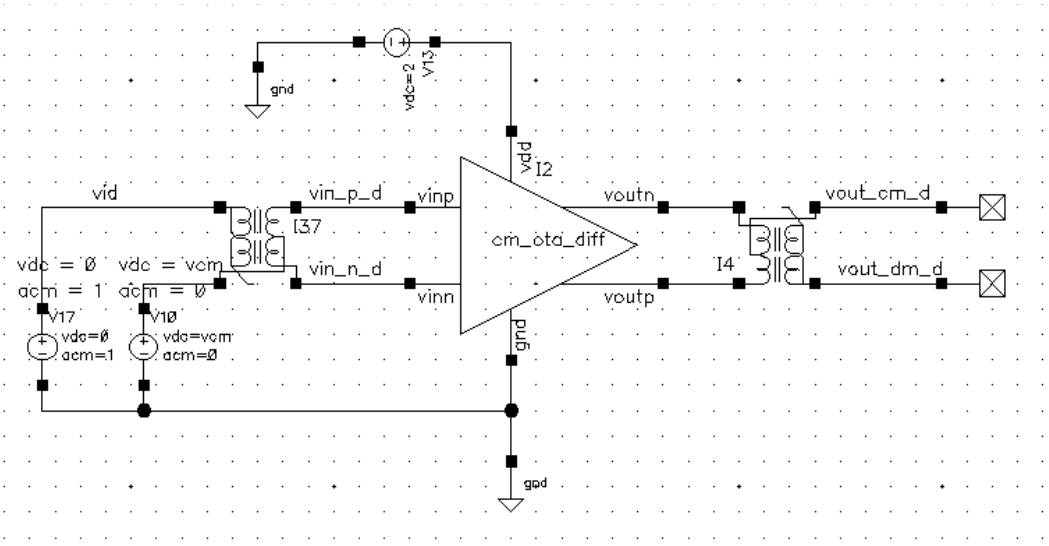

Figure 4.7: Common Mode Rejection Ratio Testbench - Differential Mode Configuration.

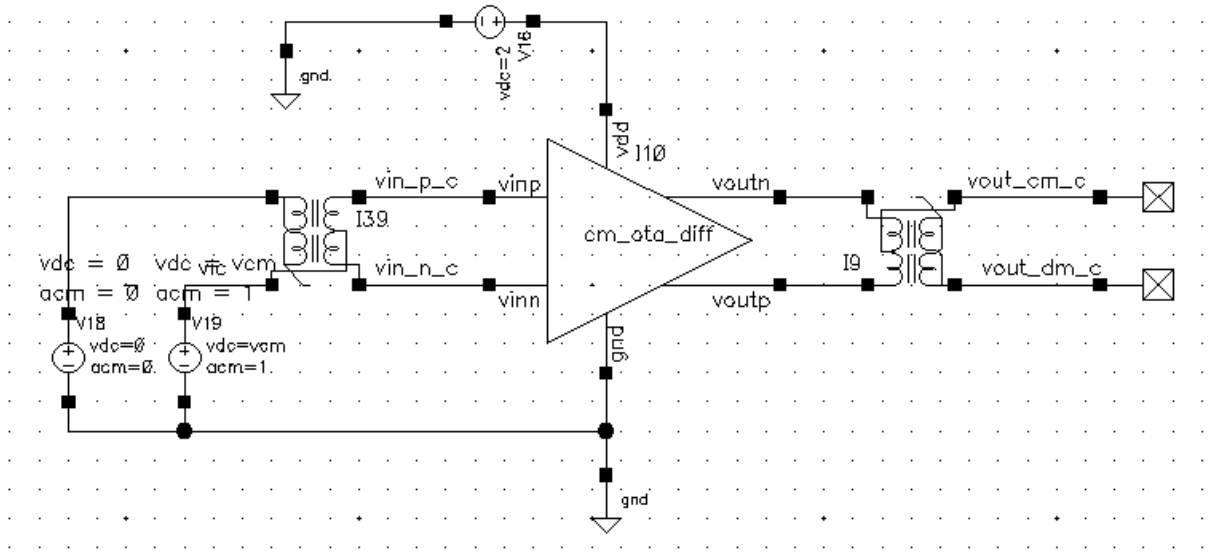

Figure 4.8: Common Mode Rejection Ratio Testbench - Common Mode Configuration.

5. Simulation Results

5.1. OTA Overall Gain / Bandwidth / Phase Margin

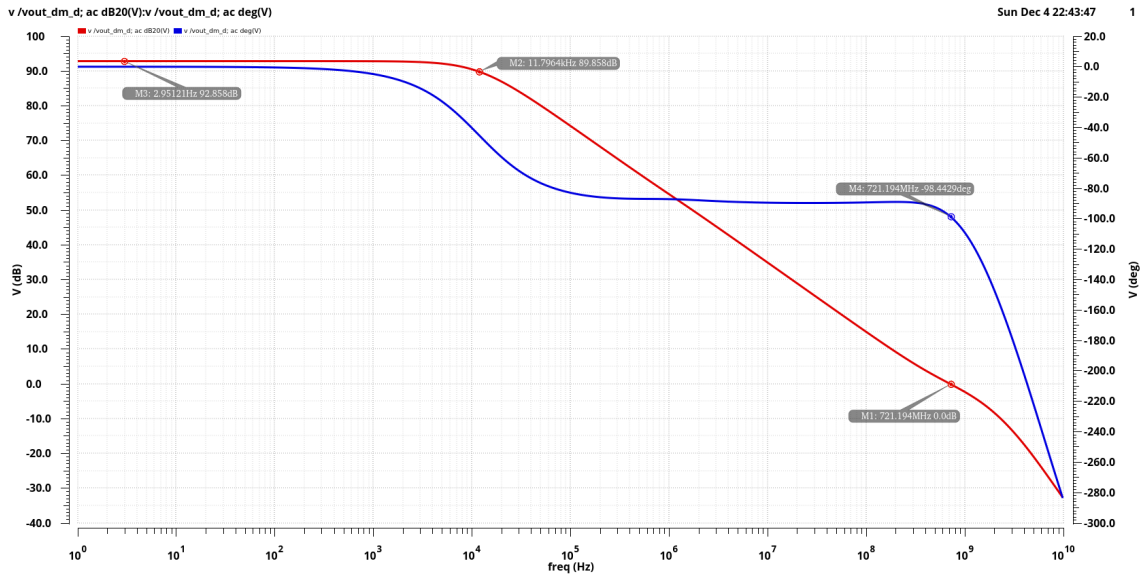

Figure 5.1: Magnitude and phase of the overall OTA.

5.2. Internal Feedback Loops Gain and Phase Margin

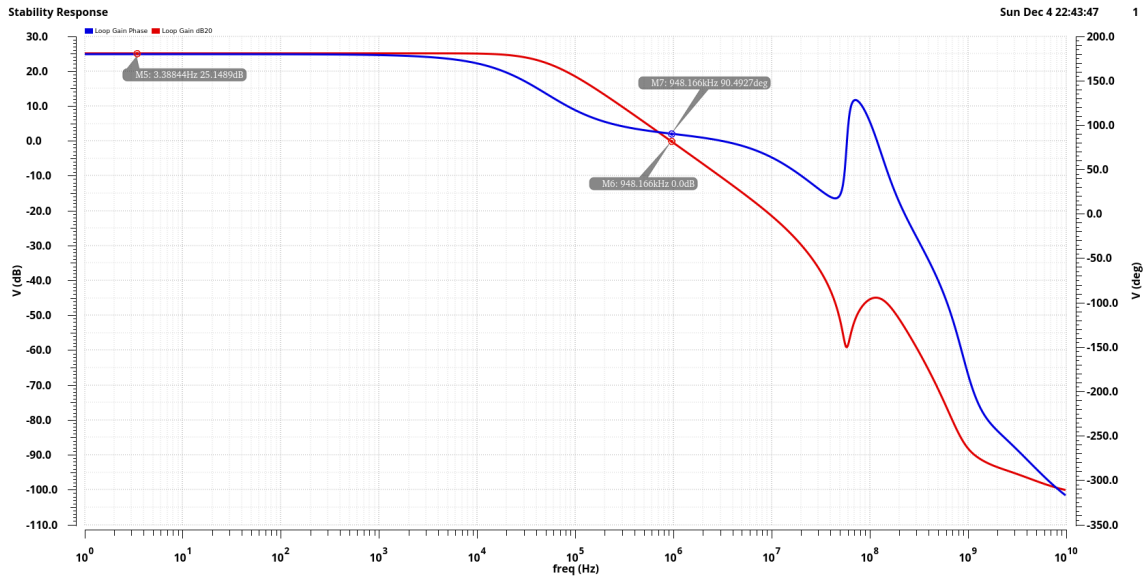

Figure 5.2: Gain and Phase of PMOS Active Cascode. Same for both legs.

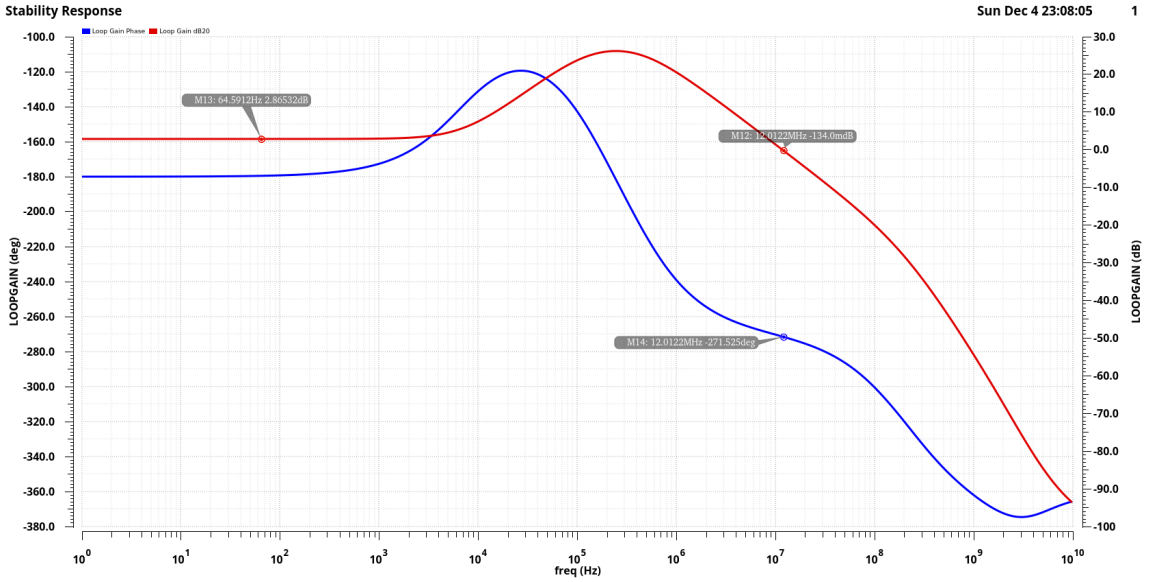

Figure 5.3: Gain and Phase of NMOS Active Cascode. Same for both legs.

5.3. Common Mode Feedback Loop Gain and Stability (PM)

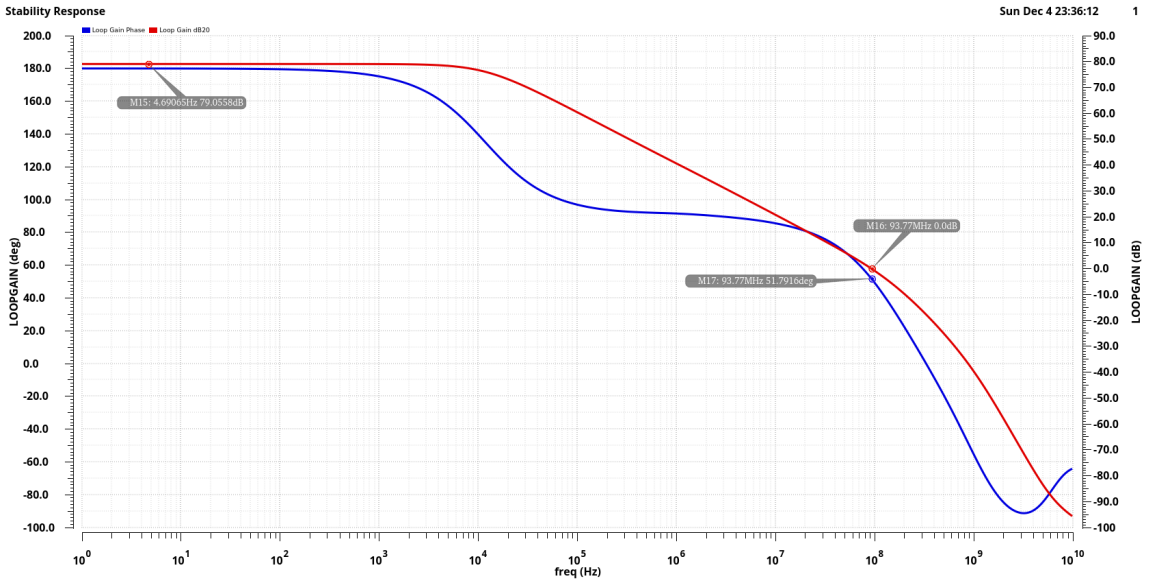

Figure 5.4: Loop gain and phase of the Common Mode Feedback for the OTA.

5.4. Settling Time and Slew Rate

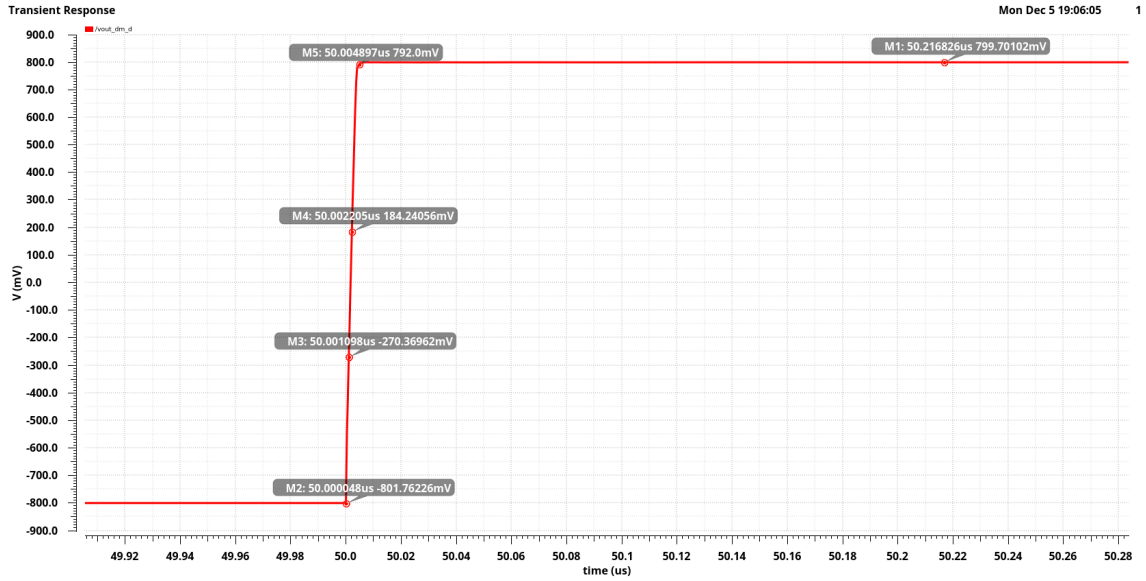

Figure 5.5: Step transient response of the OTA to determine settling time and slew rate.

5.5. Input Common Mode Range

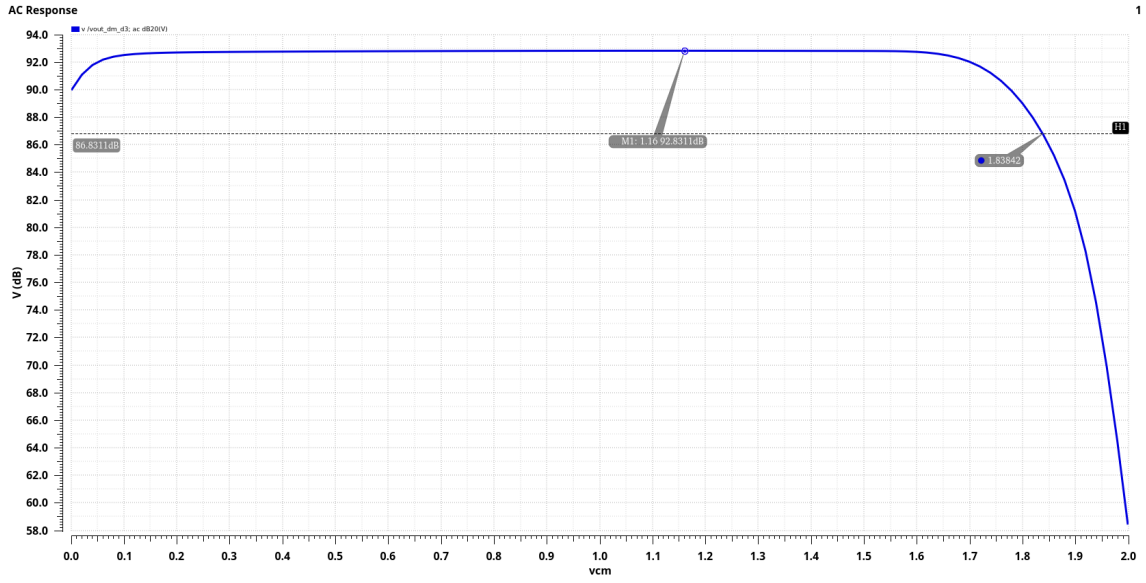

Figure 5.6: DC/AC sweep of the input common mode range.

5.6. Output Swing

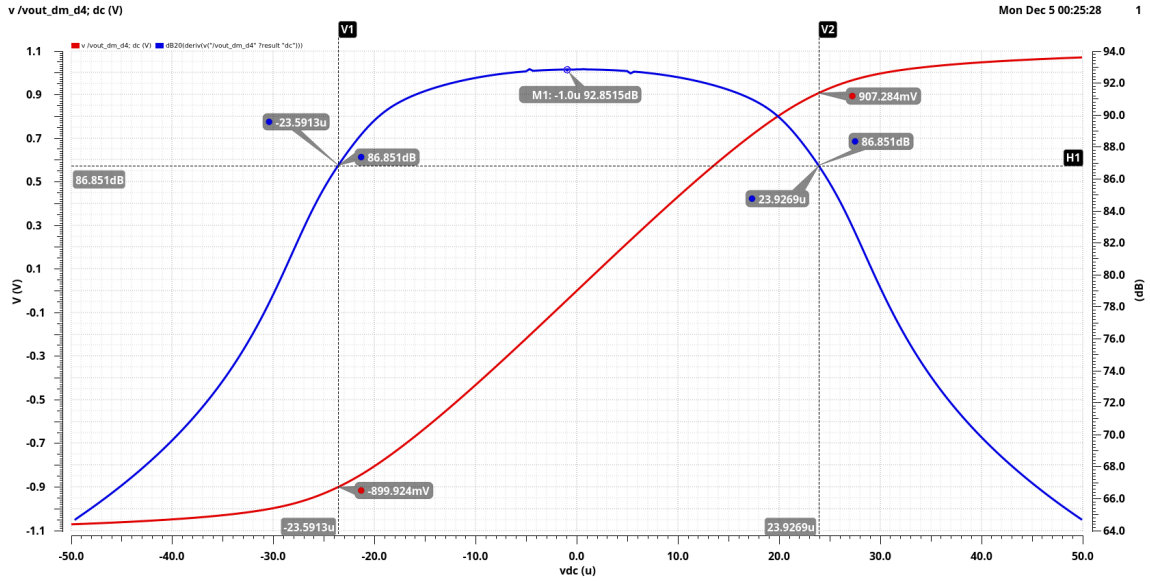

Figure 5.7: DC/AC sweep of the output range.

5.7. Common Mode Rejection Ratio

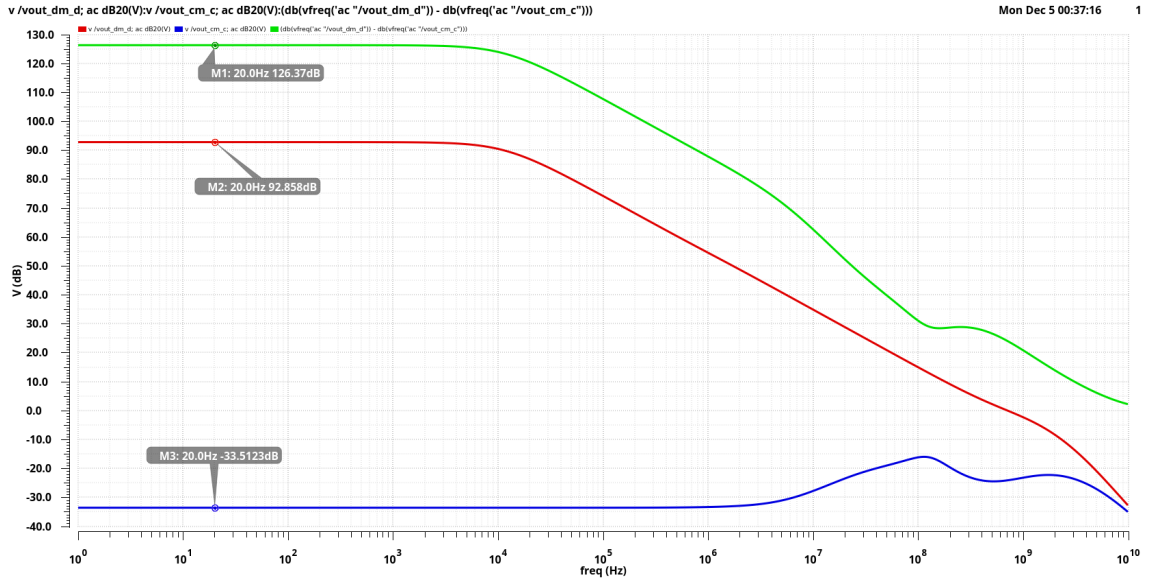

Figure 5.8: Differential mode gain, Common mode gain, and Common Mode Rejection Ratio (CMRR).

5.8. Power Supply Rejection Ratio

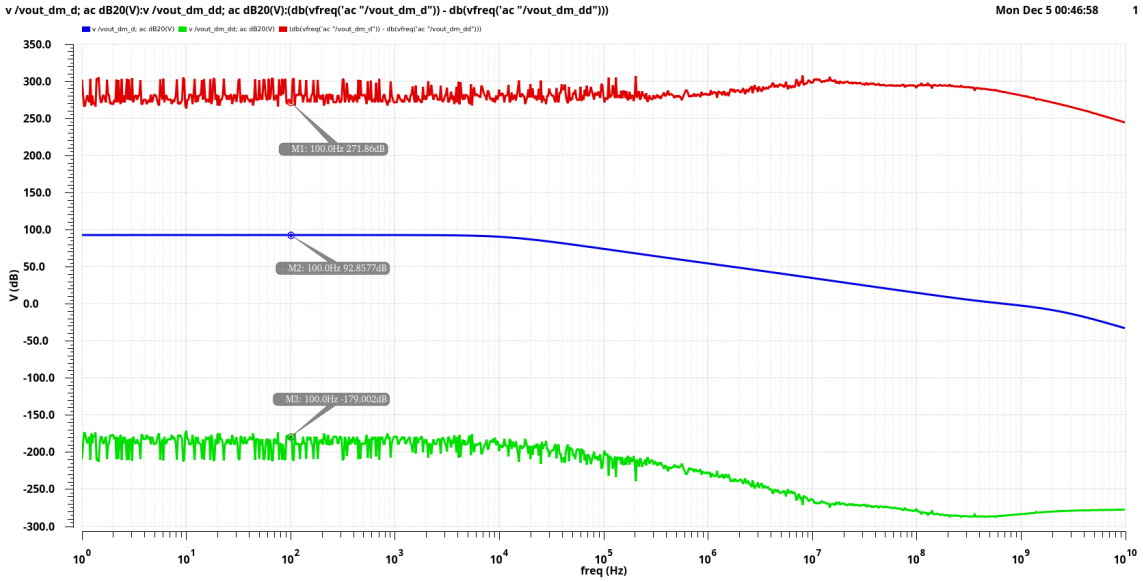

Figure 5.9: Power Supply Rejection Ratio (PSRR).

5.9. Input Equivalent Noise Voltage

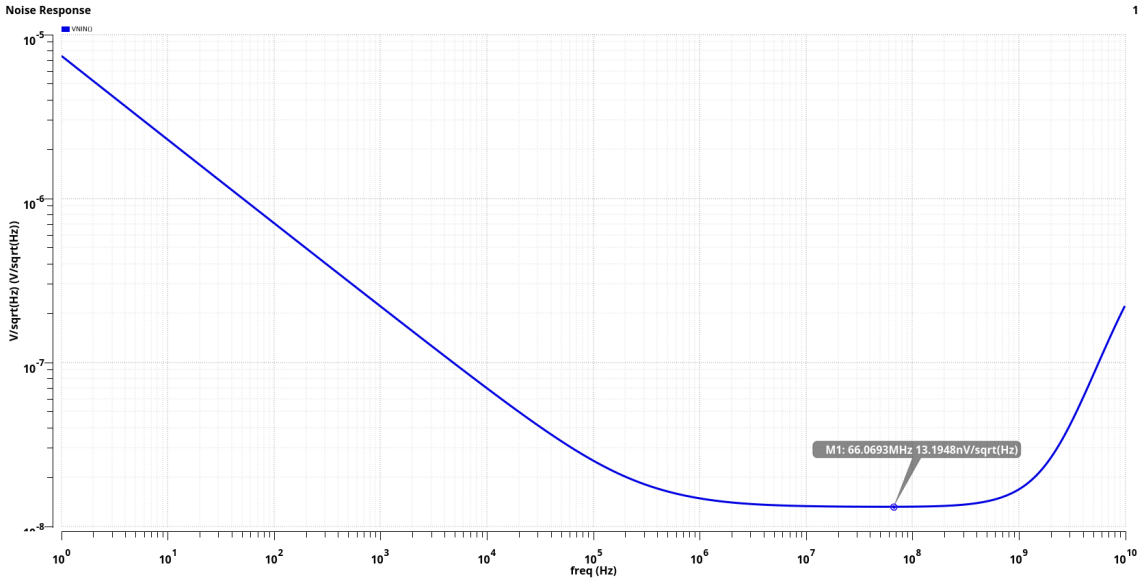

Figure 5.10: Noise analysis of the OTA. Marker highlights the Noise floor of the circuit.

6. Conclusion

Overall, the design meets a majority of the requested specifications of the project with the exception of Common Mode Feedback phase margin, the output swing, and the input-referred noise voltage floor. With more time, the bias generator would be optimized to redirect current from these circuits onto the tail current of the main OTA. Allocating more current to these areas can improve the phase margin and slew rate due to increasing the input leg Gm. A potential avenue of reducing the current requirements within the biasing circuitry would be to reduce the amount of parallel branches that are sourcing current to produce voltages by potentially “daisy chaining” one branch with multiple MOSFETs. These MOSFETs (by their W/L ratio or other means) can be optimized to produce multiple biasing voltage for one branch of current. This would require much more time to fine tune the circuit with multiple PMOS circuits in conjunction with the NMOS cascode current mirror to produce multiple usable voltages for every branch.

With more time, the output swing would be addressed by investigating CMFB operation. The device sizing and biasing was not analyzed in depth as this aspect was left till the last minute, without awareness of its utmost importance.

Inadvertently, throughout the design process, only the phase margin of the overall circuit was considered. This drove the decision making and diverted focus away from other subcircuits such as the NMOS active cascodes. With more time, the low loop gain observed in the NMOS Active Cascode amplifier would also be addressed.

Noise for the circuit could have been decreased by increasing the capacitance of the circuit and reducing the resistances within the circuit itself which would have generated issues with the phase margin from compensation, gain and transient analysis along with the voltage biasing [5][6].

Overall the OTA design works well. Some tradeoff choices had to be made and this is apparent in the specifications that were met well and the other specifications not met. If more time had been available after the realizations of mistakes made with CMFB and with a stronger understanding of compensation, these design issues might have been carefully probed and resolved. The next steps that would be pursued would be to carefully understand and test the operation of the NMOS active cascode and CMFB circuits.

Appendix: Schematic Set 2

A.1. Overall Schematic with Hierarchy

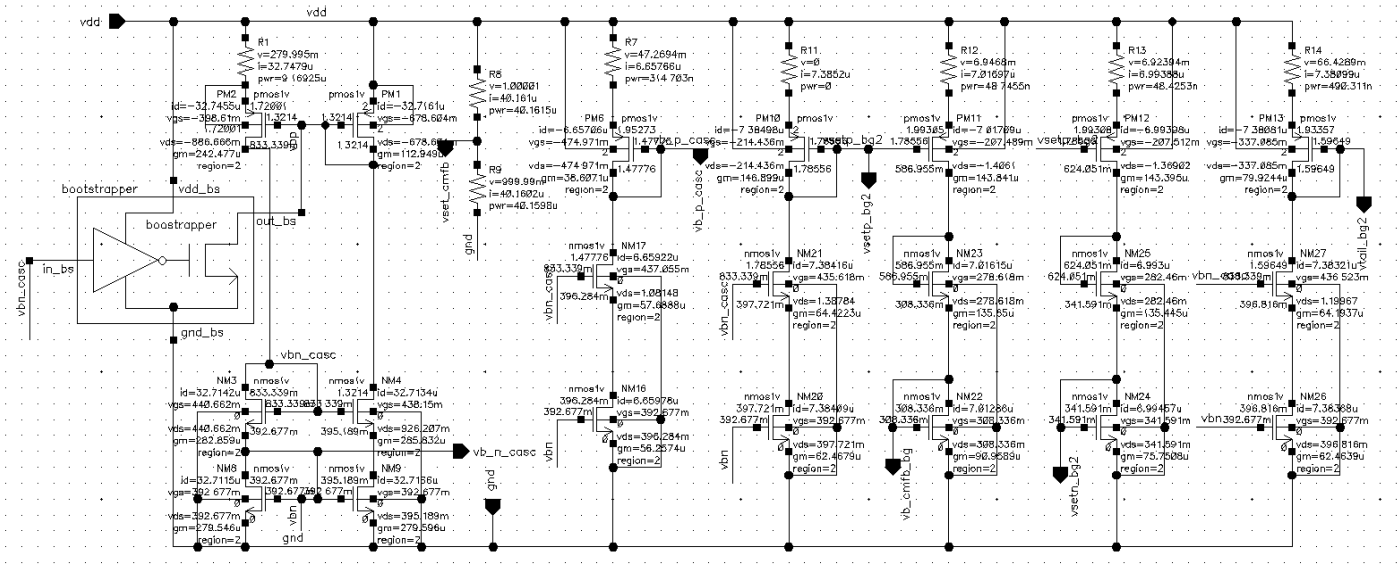

Figure A.1: High Level Design of the OTA.

A.2. Active Cascodes

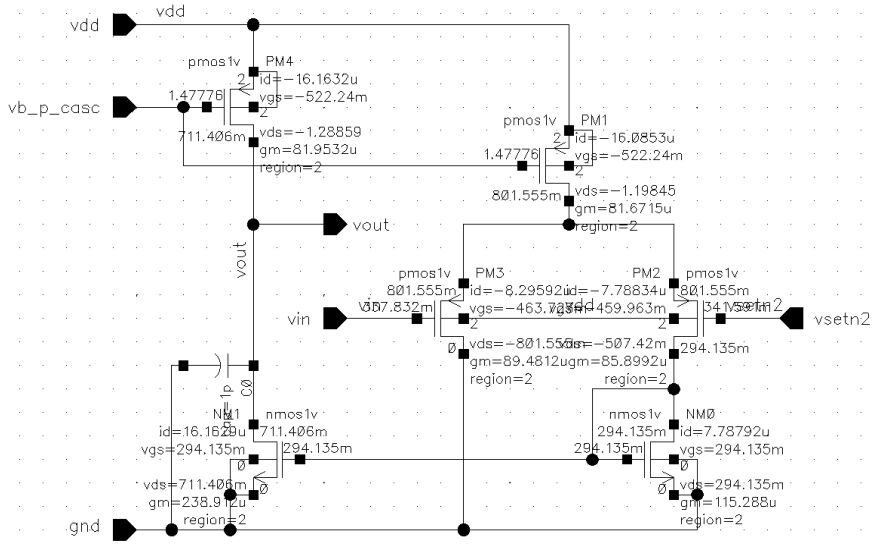

Figure A.2: Schematic of the NMOS active cascode circuit.

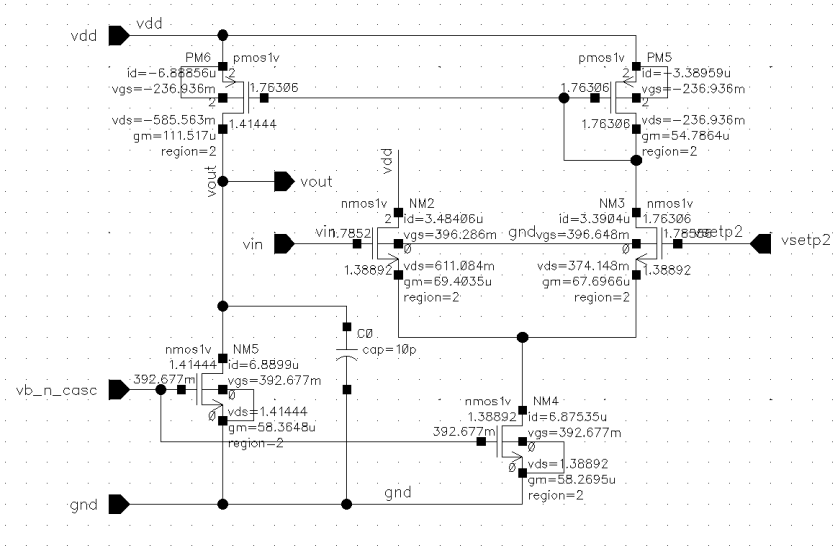

Figure A.3: Schematic of the PMOS Active Cascode Circuit.

A.3. Common Mode Feedback (CMFB)

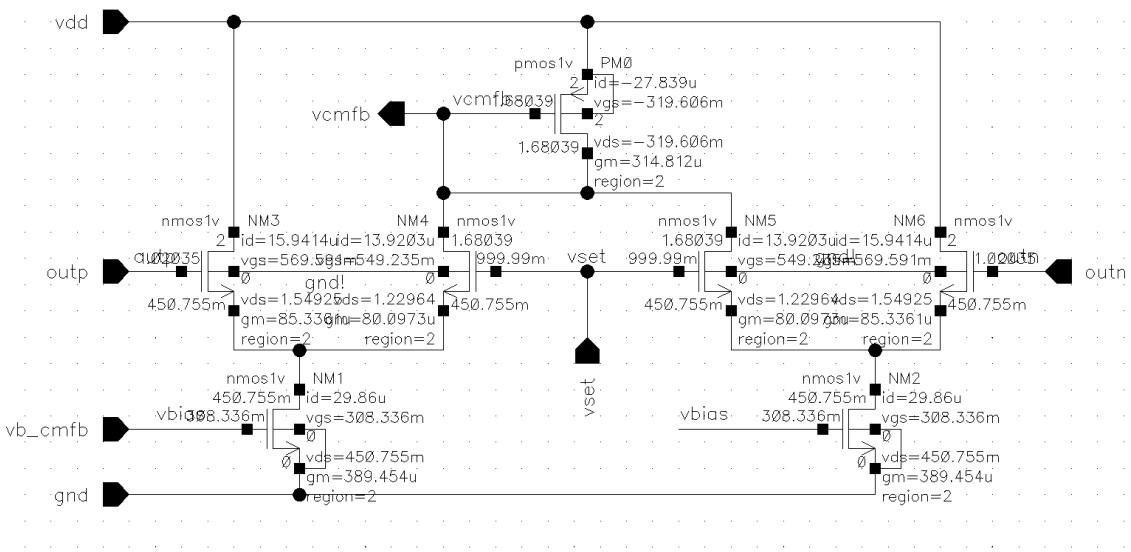

Figure A.4: Schematic of the CMFB Circuit.

A.4. Constant g_m Biasing Circuit

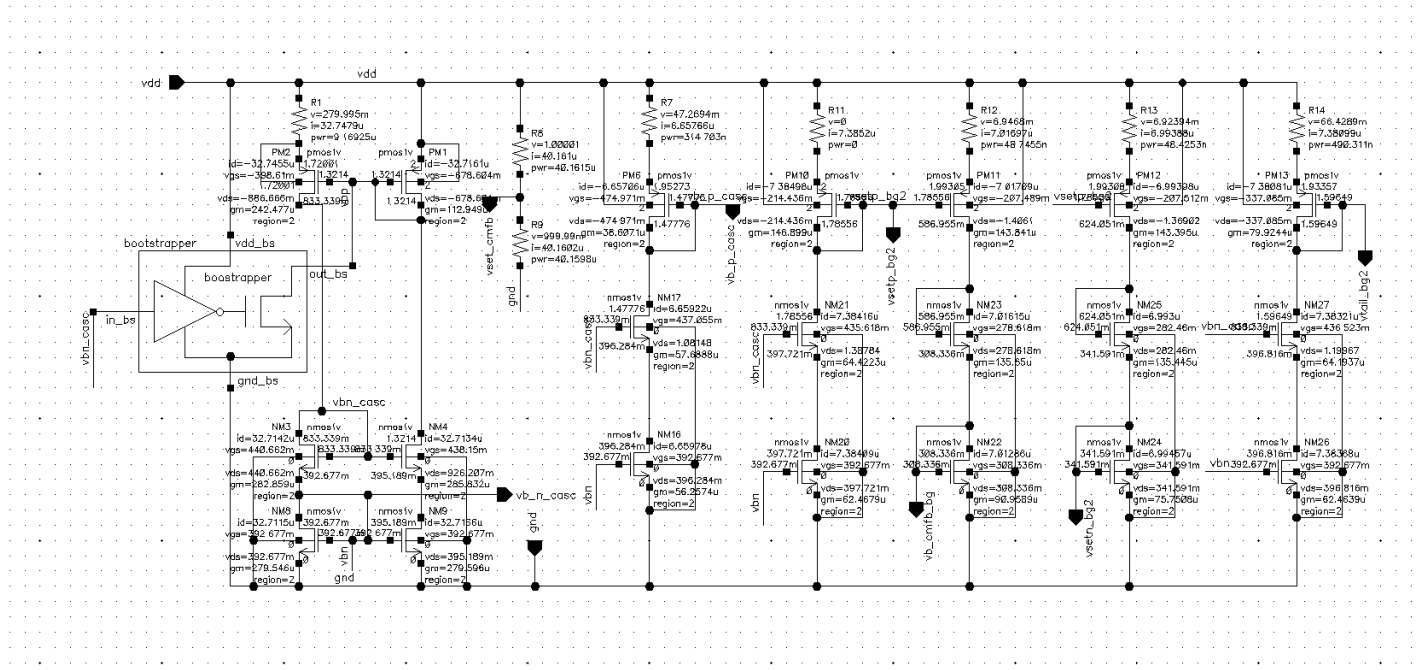

Figure A.5: Schematic of the Constant g_m Biasing Circuit.

A.5. Bootstrapping Circuit

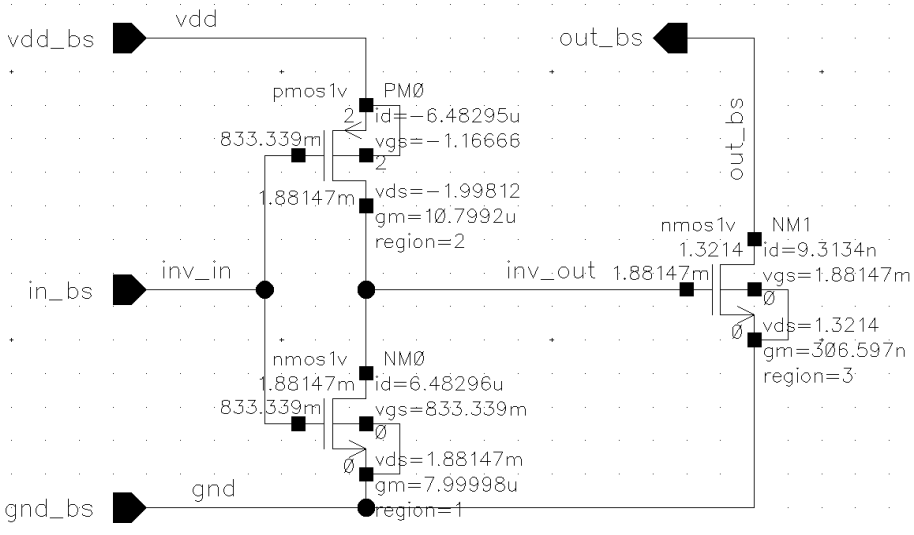

Figure A.6: Schematic of Bootstrapping Circuit.

A.6. Test Bench

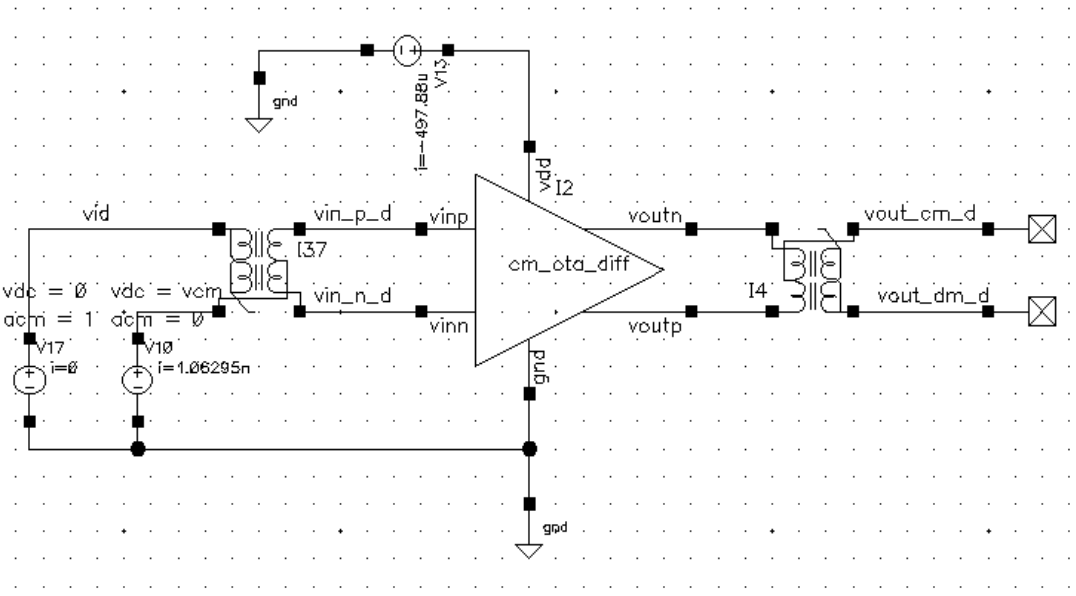

Figure A.7 *Common Mode Rejection Ratio Testbench - Differential Mode Configuration.*

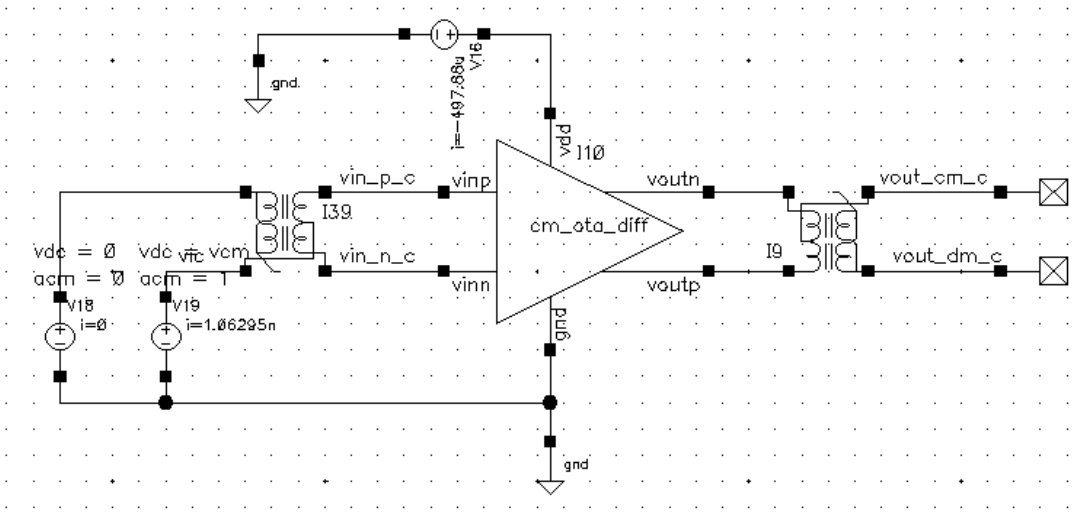

Figure A.8 Common Mode Rejection Ratio Testbench - Differential Mode Configuration.

References

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